Synthesizable Implementation of 2N/N Binary Division

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The paper introduces a synthesizable implementation of 2N/N integer division, addressing the need for efficient hardware realization of division operations in digital systems. Traditional division circuits often suffer from high resource utilization and long latency, making them unsuitable for realtime applications. The proposed implementation leverages Cadence tools and methodologies to optimize hardware resources while ensuring high performance and low latency. Current restoring dividers often face computational overhead during iterative restoration, motivating the need for improved methods. The proposed technique utilizes a multiplexer to restore the original dividend bits when the subtraction result is negative, ensuring division accuracy. This approach aims to balance precision and computational efficiency by introducing controlled errors using an approximate adder. Future avenues for refinement include fine-tuning error tolerance and exploring alternative approximation techniques for better efficiency. Addressing these aspects will advance the proposed method's effectiveness and applicability in practical computing environments.

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