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# An Efficient Implementation of AES Algorithm for Cryptography Using CADENCE

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**Abstract:** Modern-day technological advancements have led to the increasing amounts of data being transmitted and received. Security, being one of the major concerns, several data encryption algorithms have been employed to protect the data from fraudulent usage. Out of the several algorithms, AES has been widely accepted for providing higher degree of confidentiality and simplicity in implementation. Several modifications have been suggested by researchers in enhancing the security of this algorithm. This work presents a novel technique for dynamic S box generation in AES cryptography. The module used for key expansion of the AES implementation is modified to reduce the power consumption and the area occupied by the structure. The proposed method of implementation using NAND gates can be used in FPGAs for reduced power consumption. This work presents a novel method for implementation of AES cryptography hardware implementation and its power consumption. The proposed method of implementation using NAND gates can be used in FPGAs for reduced power consumption.

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