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Stability analysis of improved combined-mode power converter and power flow control using FPGA

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ABSTRACT

An improved combined-mode power converter (CMPC) for a solar photovoltaic (SPV) system is presented in this paper. Ten-power electronic switches are utilised for the functioning of the converter. The proposed converter has four modes of operation: buck, boost, inverter, and mixed mode. The new CMPC topology provides a unique and complex switching sequence for implementing the mixed-mode operation. This work uses a field-programmable gate array (FPGA) for mode selection and to create PWM (MS-PWM) signals. A digital MS-PWM controller is configured to switch between improved stepped perturb and observe (ISPO) maximum-power point tracking (MPPT) and sine wave PWM (SPWM). The ISPO provides the appropriate duty cycle for buck/boost operation, while the SPWM controls the inverter operation. This work's new digital PWM control algorithm supports mode selection, PWM generation, and reconfiguring PWM generation timings. The whole framework for constructing the MS-PWM controller employs a very high-speed integrated circuit hardware description language (VHDL). Simulation and experimental results are presented, proving that the digital MS-PWM controller uses fewer resources with improved accuracy.