Performance Analysis of FPGA Implementation of 4 x 4 Vedic Multiplier using different adder architectures

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High-speed applications, such as signal processing and image processing, require fast computations, which in turn require high-speed multiplications. Multipliers are the most essential components in signal processing systems and are used for various operations such as filtering, modulation, coding, and decoding. Therefore, the development of high-speed multipliers is crucial for meeting the demands of modern digital signal processing applications. There are various techniques used to design high-speed multipliers, such as parallel multipliers, array multipliers, and carry save multipliers. These techniques help in producing fast and efficient multipliers that are capable of meeting the demands of high speed applications. The multiplier blocks are considered as one of the major hardware blocks causing a bottleneck in terms of power dissipation and delay in most of the fast processing systems. Multiplication operation consumes high power and more hardware resources when compared to other arithmetic operations. This paper highlights the design and FPGA implementation of 4-bit Binary Vedic multiplier, which results in less power dissipation and low propagation delay when contrasted with conventional type of multipliers. The simulation of the vedic multipliers is carried out using Xilinx 2018 software with the HDL Verilog. The design is implemented and synthesized using FPGA board (Zed board). Also, the output is visualized using the board The performance analysis is conducted for the Vedic Binary multiplier designed with various adder architectures.

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