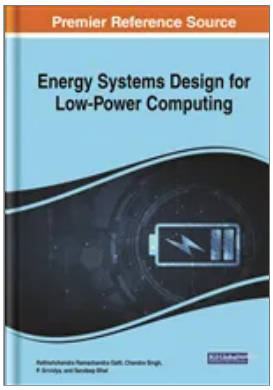

An Enhanced Method for Running Embedded Applications in a Power-Efficient Manner

N. M. G. Kumar (/affiliate/n-mg-kumar/439645/), Ayaz Ahmad, Dankan Gowda V., S. Lokesh, Kirti Rahul Rahul Kadam

Source Title: Energy Systems Design for Low-Power Computing (/book/energy-systems-design-low-power/293050)

Pages: 21

DOI: 10.4018/978-1-6684-4974-5.ch013

Abstract

Many modern items that are in widespread use have embedded systems. Due of embedded processing's ability to provide complex functions and a rich user experience, it has grown commonplace in many types of electronic products during the last 20 years. Power consumption in embedded systems is regarded as a crucial design criterion among other factors like area, testability, and safety. Low power consumption has therefore become a crucial consideration in the design of embedded microprocessors. The proposed new method takes into consideration both the spatial and temporal locality of the accessed data. In the chapter, the new cache replacement is combined with an efficient cache partitioning method to improve the cache hit rate. In this work, a new modification is proposed for the instruction set design to be used in custom made processors.

Chapter Preview

Top

Introduction

An Embedded system is a combination of an electronic and a computer system. It is a computer or processor-based system designed to perform a dedicated sequence of the task to control or operate a large system (mechanical or electrical) with real-time constraints. It is a system used to perform its functions without human intervention completely or partially. It is

also designed to accomplish a particular task in an efficient method. Mostly, embedded systems are used in operation where timing is very important (Aaron Lindsay and Binoy Ravindran. 2018). In the modern-day embedded systems applications, battery operated devices play an important role. The applications that run on those embedded devices rely more and more on powerful processors and are capable of running real-time applications. Because of the increase in number as well as the complexity of such applications, a significant amount of work has focused on the minimisation of power and energy consumed by the embedded processors (Chen Yang and Leibo Liu. 2018). Apart from giving a result in real-time, these embedded devices are to be designed to satisfy thermal limits as well as battery life limits, thereby directing the research towards low power and low energy enhancements. Along with performance, ease of use, and other such design metrics, power consumption is also a design metric for the present-day embedded systems. Embedded applications are demanding more processing power along with the ever-increasing need for more memory. It calls for active research to satisfy this multiple objective design challenge to develop an application for multicore embedded systems and their memory managing capabilities. The power consumption happening in memory by static and dynamic leakages is calling for a need to work on relevant solutions (Chenjie Yu and Peter Petrov. 2019). The power leakage in the bus and memory also create other side effects on the processor like thermal effects.

The cache contention happening in multicore processors can be addressed by the cache partitioning scheme to maximise the cache space utilisation. It may also increase the execution timing of the task. This work proposes a priority-based cache partitioning approach among the cores to improve both the cache performance and deadline avoidance. An embedded systems benchmark is used to select the set of applications from workloads to work on this cache partitioning problem (Dan, A and Towsley. D. 2020).

This work also presents a method to reduce the power consumed in the instruction fetching data bus during the execution of the instruction. The instruction code fetched from memory is modified so that the bus is loaded less, and therefore the switching capacitance associated with the bus is reduced(Daniel Sanchez and Christos Kozyrakis. 2021). This results in decreasing the power consumed in the data bus during the instruction fetch cycle. To explore a working cache model for a multi-core processor with configurable cache details and to incorporate run time cache optimisation for power minimisation.

The research problem of improving cache design in the context of power and energy optimisation is important because, in today's processors, the cache memory has a share of over 30% of the total processor's power. Cache memory, which is accessed faster and also with a good hit rate, is considered to be more power-efficient (Dimitris Kaseridis and Jeffrey Stuechelix. 2009). By selecting a better cache replacement algorithm which can be implemented either as hardware maintained structure or as a program (Dongwoo Lee and Kiyoung Choi. 2019). This method reduces the bus power of the processor during program execution. Power consumption in embedded systems is one of the important issues. Since a substantial amount of power consumption in a processor happens inside the cache and memory operations. this chapter proposes a technique on that domain to reduce the power consumption in embedded systems

Complete Chapter List

Search this Book: Full text search terms

Reset