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Implementation of Linear Test Stimulus Generator for Non-linearity Computation of ADC

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Abstract

A linear ramp stimulus is generally preferred to accurately measure the non-linearity errors in an analog to digital converter (ADC). Three methods are proposed to generate a linear ramp signal, of which the first approach employs two sine waves. In contrast, the second utilizes a sine wave with a pulse signal to generate a parabolic signal which is then differentiated to produce a ramp signal. The third method achieves linearity by maintaining a constant potential across the resistor to push a constant current into the capacitor. The three proposed concepts have been designed and simulated to compute the differential non-linearity (DNL) error for an ideal 8 bit ADC in 90 nm CMOS technology. The third method shows high linearity when compared to the existing methods, by exhibiting a very low DNL error of 0.0015 LSB in simulation. Its implementation indicates that 92% of the silicon area is reduced, making it suitable for ADC testing.