

Analytical Modeling of Junctionless Accumulation-Mode Triple-Material Surrounding Gate Nanowire (JATMSG) Transistors Using Fourier–Bessel Transform



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Abstract An analytical model of a new device called junctionless accumulation-mode triple-material surrounding gate (JATMSG) nanowire transistors is presented for the very first time using a different approach. The doping concentration and the charge concentrations are taken into consideration, and the method is a quite easy approach of Poisson equation and its solution using Fourier–Bessel function method. The device performance is investigated through the analysis of the parameters central potential and electric field for various parameters, and the results are simulated using TCAD tool. The results align well with the software simulation results.

Keywords Junctionless transistors · Surrounding gate · Nanowire · Potential

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1 Introduction

In the miniaturized electronics era, more than Moore's Law, the transistor size is scaled and used in various modern applications [1, 2]. This also pronounces negative effects called short-channel effects (SCE). In order to exempt and reduce the so-called SCEs, devices are modified in different forms and one such modification is gate engineering, i.e., having more than one gate material. Even though many devices are proposed in this umbrella, the triple-material gate is not much discussed in recently emerging junctionless devices. This paper presents the analytical modeling of the junctionless accumulation-mode triple-material surrounding gate nanowire (JATMSG) MOSFETs. The junctionless transistors are newly emerging candidate which has uniform doping concentration throughout the device. The fabrication process is simpler than the junction devices. The conductivity of the device has to be increased, and hence, it employs heavily doped channel. This process produces an effect of reducing the carrier mobility, thereby decreasing the carrier transport value. These factors tend to increase the SCEs, specifically drain-induced barrier lowering (DIBL). This paper aims to reduce the DIBL, and hence, triple-material gates with different work functions are chosen. The provision of the triple-material gate will produce a step-up curve in the potential, thereby screening the device from SCEs.

For scaling the device further, it is essential to reduce the short-channel effects, and hence, an efficient model has to be developed which also points out the accumulation mode of the device along with the SCEs. Even though many models are available for predicting the characteristics of the device, they are based on the 1D Poisson equation [3–12] focusing on the long-channel device. Also, the classical model develop is applicable only for devices whose silicon thickness is equal to 5 nm. There is no specific model focusing only on the SCEs. The drawback with the existing methods is exposed when the oxide thickness between the source and the gate is reduced [13–19]. This paper showcases the analytical model derived for the junctionless accumulation-mode triple-material surrounding gate nanowire MOSFETs and obtains the central potential and electric field, analyzing the short-channel characteristics of the device. The results are validated using the TCAD tool.

2 Device Structure

The cross-sectional view of the proposed device whose gate length is 100 nm is shown in Fig. 1. The triple-material gates also section the channel into three regions. The modeling is carried out in three regions separately using three different equations. For consideration, the source and drain regions are located on either side of the heavily doped channel. The model is developed assuming the following Poisson equations given in Table 1.

Table 3 Comparison of electric field

Authors	References	Device specification (Junctionless)	Method	Electric field values (X 105) for the channel position				
				0.1	0.3	0.5	0.7	0.8
Tripathi et al.	[32, 33]	Triple-material	Simulation	− 1	− 3	− 1	− 3	− 1
Pathak et al.	[34]	Graded-channel dual-material	Simulation	− 0.5	− 3.5	− 2	− 0.5	− 2
Baruah et.al	[35]	Dual-material with high K	Simulation	0.5	2	3.5	2	1.5
Preethi et al.	[36]	Dual-material	Finite differentiation method	0.2	0.3	0.6	0.5	0.4
Misra et al.	[38]	Graded-channel single-material	Simulation	0.6	0.8	1.1	0.8	1.0
Proposed device			Fourier–Bessel transform	− 0.5	0.2	− 0.01	0.2	0.1

4 Conclusion

This paper investigates the potential characteristics of junctionless accumulation-mode triple-material surrounding gate (JATMSG) nanowire transistors. The device is analytically modeled, and the central potential is derived using superposition theorem. The central potential is analyzed for various drain bias, gate length ratios, and oxide thickness and compared with the existing conventional JADMSG and JASMSG transistors. The performance is also extended to derive the electric field of the device. The illustrations show the variation, and the reasons are discussed in detail. This further paves a way to scale the device further, thus providing measures to reduce the SCEs.

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