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ORIGINAL RESEARCH

High-efficiency multilevel inverter topology with minimal switching devices for enhanced power quality and reduced losses

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Abstract

The advent of multilevel inverters (MLIs) has brought significant advancements in their applications across industrial, residential, and renewable energy sectors, as they produce high-quality output voltage that closely approximates a sinusoid in small voltage steps or levels, resulting in lower total harmonic distortion (THD) and reduced electromagnetic interference (EMI). However, the MLI topologies require more switching unidirectional/bidirectional semiconductor devices with high standing voltage, gate drivers, and complex control strategies while attaining higher voltage levels. From this perspective of reducing component count and gate drivers, the objective is to develop a new MLI topology that overcomes the drawbacks above. In this article, a novel MLI topology is introduced in symmetric and asymmetric configurations aiming to attain fewer power electronic devices for synthesizing more steps in the load voltage in contrast with conventional topologies. The idea behind the approach is coining the series connected voltage source, which imbibes bidirectional current flow with an additional voltage source for performing algebraic operation under asymmetrical modes of operation. The proposed topology uses minimal on-state switching devices leading to a diminution of power loss and voltage drop. The suggested topology is optimized for a fewer number of power devices, an input DC supply, and auxiliary gate drivers to achieve a maximum voltage level in the load terminals. The suggested topology has been verified in SIMULINK and the laboratory prototype is constructed in line with the simulated response to demonstrate its performance suitable for real-time applications.

1 | INTRODUCTION

Multilevel inverter (MLI) plays a vital part in modern power electronics because of their significance such as improved power quality, high voltage capability, enhanced efficiency than modularity, and scalability [1–3]. The topologies addressed in [2] overcome the major issues for conventional fault-tolerant MLI topologies taken into account diminishing the device count retaining output power at the time of faults, enduring switch failures at any fault location, managing single or multiple switch failures and achieving the capacitor voltage balancing in the inverter. A new switched-capacitor-based boost multilevel inverter topology (SCMLI) has been designed with nine fast-switching high-frequency switches with two capacitors and a single DC source to attain nine-level output voltage. The basic configuration could be designed with two additional switches to acquire the required high-voltage gain for real-time applications. M. D. Siddique et al. [3] have presented a configuration under parallel operation which claims a self-voltage capacitor, reduced switch, and inherent polarity reversal capability. In renewable

energy applications and modern automation industries with AC drives, several remarkable topologies play an important role [4–6]. A traditional switched-diode structure has three power switches or diodes and DC voltage sources to produce five positive voltage levels. By combining multiple instances of this basic topology, two new cascaded configurations have been introduced to upgrade the voltage levels with minimum power switches. The conventional MLI configurations such as neutral point diode clamped (NPDC), flying capacitor (FC), and cascaded H-bridge inverters (CHB) [7–9] have been discussed. The recommended topology has been configured with four input DC sources and nine switching devices to form an asymmetrical voltage source configuration, enabling the generation of 17 voltage levels. By cascading multiple instances of this topology, the voltage levels could be increased with less voltage strain on the switches without changing the design. Multilevel inverters enhance the power quality by producing a more refined load voltage waveform than conventional two-level inverters. To achieve this optimized sinusoidal output voltage waveform, this configuration requires additional isolated DC power sources and DC-link capacitors. Due to these reasons, the multilevel inverter design cost increases and requires a refined control algorithm to operate the inverter. The H-bridge inverters are widely utilized in AC drives because of their fault-tolerant recovery ability, modular design, and immunity to capacitor voltage balancing problems. Despite that, it possesses certain drawbacks specifically having more components and complex control with higher initial and maintenance costs, uneven voltage distribution, and bulky design. E. T. Maamar et al. [10] have designed an improved single-phase MLI for asymmetrical operation with 4 DC voltage sources and 10 MOSFET switches to generate a 21-level AC output. It is noticeable that internal fault can be sustained by the MLI retaining the maximum output voltage, and the faulty H-bridge can be replaced easily; it is easier to pump back as the inverter operates at the same voltage level. Several innovations have been made by researchers for the past two decades to overcome the drawbacks mentioned above [11–20]. A new single-phase nine-level inverter is designed which requires fewer switches to boost the DC-link voltage. In addition to the boosted voltage, the strain on the power devices remains low with all switches and diodes could be clamped by capacitors thus achieving reduced overall power loss [11]. A new topology of MLI has been devised in [12] to diminish the switching devices compared with CHBMLI. However, the structure requires more blocking diodes when the steps in the load voltage are increased. The structure requires a higher count in input DC sources to get a higher count of voltage steps which intricate both the structure and switching control system. Another topology with the same arrangement of DC sources as in [12] requires several bi-directional devices with high blocking voltage capability which restricts the inverter usage for high-voltage applications [18]. A new cascaded topology using a high-frequency DC-link to eliminate isolated DC sources is developed to produce a stepped voltage waveform. It requires a complicated magnetic circuit component design [21]. An inverter with cascaded connection of buck voltage modules has been developed to eliminate shoot-through issues, and it requires fewer inductors compared to traditional ones for current sharing among the modules [22]. A zigzag arrangement of DC sources reduces the switching counts compared with CHB MLI, but the topology has a lesser impact on fault-tolerant operation [23]. The topology cited in [24] is simple in structure and is derived from recently proposed topologies. However, it requires more voltage sources to achieve more voltage steps and is unable to operate under device failure conditions. A novel topology has voltage sources switched at parallel/series operation to synthesize stepped voltage and the structure has switching elements in the load current path reasonably high; hence on-state losses increase when increasing the steps of load voltage [25–28]. A new 17-level switched-capacitor multilevel inverter (SCMLI) configuration has been suggested with 11 switches to achieve an elevated boost of the input voltage four times to utilize the series-parallel arrangement of capacitors with the DC voltage source. The voltage across the capacitor remains balanced through direct PWM control, under variable loading conditions. However, the SCMLI significantly reduces cost function (CF), capacitor ripple voltage, conduction losses, and voltage stress in contrast to other conventional topologies [25]. S. Kumari [27] has reported a seven-level MLI with an in-built voltage boosting feature by incorporating a soft-charged capacitor through the buck-boost operative inductor. In this design, the driver circuit complexity has been decreased with the help of half-bridge power modules, and the bootstrapping gate drivers. An inverter with a tri-dc source module cascaded with a half-bridge unit to synthesize a multilevel voltage waveform is presented, but it has the drawback of synthesizing intermediate steps in a ternary voltage ratio [29]. M. H. Mondol et al. [30] have developed a half-bridge cell connected to the H-6 inverter to minimize the power components; unfortunately, more power loss appears in the current path due to more switching devices. A hybrid multilevel inverter (MLI) topology based on conventional two-level inverters, offers a reduced device count compared to the traditional and many recent nine-level output voltage designs. The main task in the suggested topology is the capacitor voltage balancing which can be addressed through an optimized switching strategy. An advanced open-circuit fault detection method has been proposed which relies on load voltage waveform. It uses wavelet transform for feature extraction from the load voltage and fault classification is achieved by training an artificial neural network (ANN) [31]. A cutting-edge MLI topology has been designed with eight switches and two unequal input sources to produce an 11-level output voltage for real-time applications. By cascading this topology, the required output voltage with levels can be obtained [32]. Dewangan et al. [33] have established a new fault-tolerant multilevel inverter (FT-MLI) that can perform effectively even though open-circuit faults occur in the operating switches. It aims to temporarily meet operational requirements while reducing the component count, and a reliable fault-tolerant switching strategy combined with effective fault clearance is applied to achieve the desired output voltage [33].

In this direction, a new topology has been introduced to attain several voltage steps (or levels) using minimal standalone DC sources and power semiconductor devices with reduced

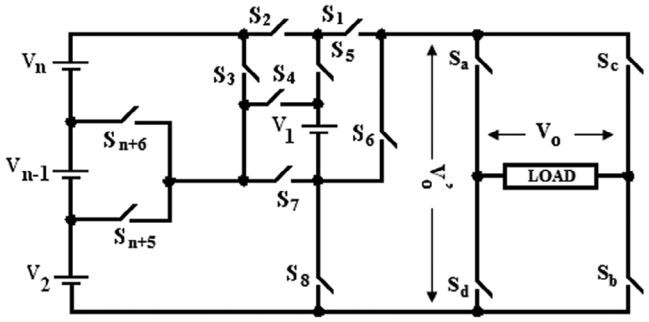


FIGURE 1 Schematic of the suggested MLI topology.

withstand voltages and energy dissipation. The conceptualized topology is constituted using a series connection of isolated voltage sources with bidirectional current flow capability to allow enhanced voltage levels. The presented topology uses an additional DC source in its structure to perform an algebraic operation for asymmetrical modes of operation reducing the total switch count about traditional and recent topologies. The envisioned topology uses a lesser switch count in the current path while enhancing the voltage levels thereby reducing power loss and total voltage level on the switches. The outlined module can be stacked to achieve enhanced voltage levels with various voltage levels. The research work is organized with a detailed study of the operating principle and its hybrid structure as presented in Section 2, and optimal topologies in Section 3 with different perspectives followed by its operation verified by simulation and laboratory results as portrayed in Sections 4 and 5, respectively.

2 | PROPOSED TOPOLOGY

MLIs foray into their path in mega-watt (MW) and high-voltage applications due to the ability to produce good quality load voltage with several voltage steps by the DC sources and DC-link capacitors with an array of switching devices. To achieve this optimized sinusoidal output voltage waveform, this configuration required additional standalone DC sources and intermediate DC capacitors. In this perspective to reduce the whole power components, a new MLI configuration is proposed as shown in Figure 1 comprising a string of isolated DC input sources (V_1-V_n = V_{IN_1}-V_{IN_n}) interfaced to the load through switches (S_1-S_{n+6}) and able to produce all possible values of V_{IN_1}. The structure produces only zero, positive values, and hence an H-bridge configuration is mandated to produce all possible voltage levels in both polarities. The voltage source (V_{IN_1}) decides the magnitude of the least step in the load voltage, and other sources (V_{IN_2}-V_{IN_n}) produce a high-level voltage step (V_{IN_1}) in the output. The switches (S_1-S_7) are effectively utilized to increase or decrease the voltage sources (V_{IN_2}-V_{IN_n}) from (V_{IN_1}-$V_{IN_}$n) in the load voltage. In this projected methodology, several isolated DC voltage sources may be accrued through PV panels or batteries. It is observed that a maximum of four switches will be conducted to add/bypass the voltage source (V_{IN_1}) with the voltage sources (V_{IN_2}-V_{IN_n}) to the load at any point in time. Consequently, the highlighted methodology requires only four switches to produce all the required voltage steps, thereby claiming fewer switching elements within the current-carrying path, and hence less power loss. The proposed topology requires (n + 10) switches to produce (2n + 1) voltage levels, where 'n' refers to total isolated DC input sources. Figure 2 depicts the modes of operation to produce various steps of load voltage. A detailed explanation of the various operating modes for extracting all the possible voltage levels is given as follows.

- **Mode 1**: To get $V_0 = V_1 = \pm V_{IN\_1}$ in the terminal voltage, the switches (S_1, S_5, and S_8) in the level generation part are to be conducted and the switch pair (S_a and S_b) and (S_c and S_d) in the polarity reversal H-bridge inverter are to be conducted as seen in Figure 2a.
- **Mode 2**: The switches (S_1, S_5, S_7, and S_9) in the level generation part are to be conducted, and the switch pair (S_a and S_b) and (S_c and S_d) in the polarity reversal H-bridge inverter are to be conducted to get $V_0 = V_1 = \pm(V_{IN\_1}+V_{IN\_2})$ in the output voltage as indicated in Figure 2b.
- **Mode 3**: The switches (S_1 and S_2) in the level generation part need to be conducted and the switch pair (S_a and S_b) and (S_c and S_d) in the polarity reversal H-bridge inverter are to be conducted to get $V_0 = V_1 = \pm(V_{IN\_1}+V_{IN\_2}+V_{IN\_3})$ in the terminal voltage as represented in Figure 2c. In this mode, only two switches are in the current conduction path, generating three times the minimum step voltage.
- **Mode 4**: The switches (S_1, S_3, S_5 and S_7) in the level generation part need to be conducted, and the switch pairs (S_a and S_b) and (S_c and S_d) in the polarity reversal H-bridge inverter must conduct to obtain $V_0 = V_1 = \pm(V_{IN\_1}+V_{IN\_2}+V_{IN\_3}+V_{IN\_4})$ in the terminal voltage as outlined in Figure 2d.
- **Mode 5**: For asymmetrical operating states of the recommended MLI, the switching devices (S_1, S_3, S_5, and S_7) are connected to the voltage sources (V_{IN_2}-V_{IN_4}) with the voltage source (V_{IN_1}) to the load as depicted in Figure 3.

Table 1 represents the power elements requirement between the proposed and the existing topologies available in the dynamic applications. Here the notation's' represents how many levels or steps are available in load voltage. Table 2 tabulates the evaluation of the recommended MLI and contemporary topologies by considering four DC sources as a basic unit (k) to get a variety of output voltage with asymmetrical voltage sources. The other hybrid form is also configured using the proposed MLI topology and an isolated H-bridge inverter, producing higher voltage steps as represented in Figure 4. These hybrid structures have many possibilities of generating a higher count of voltage steps using binary and ternary ratios. The proposed topology can be reconfigured for a hybrid configuration using either three or four voltage sources to achieve reduced blocking voltage and

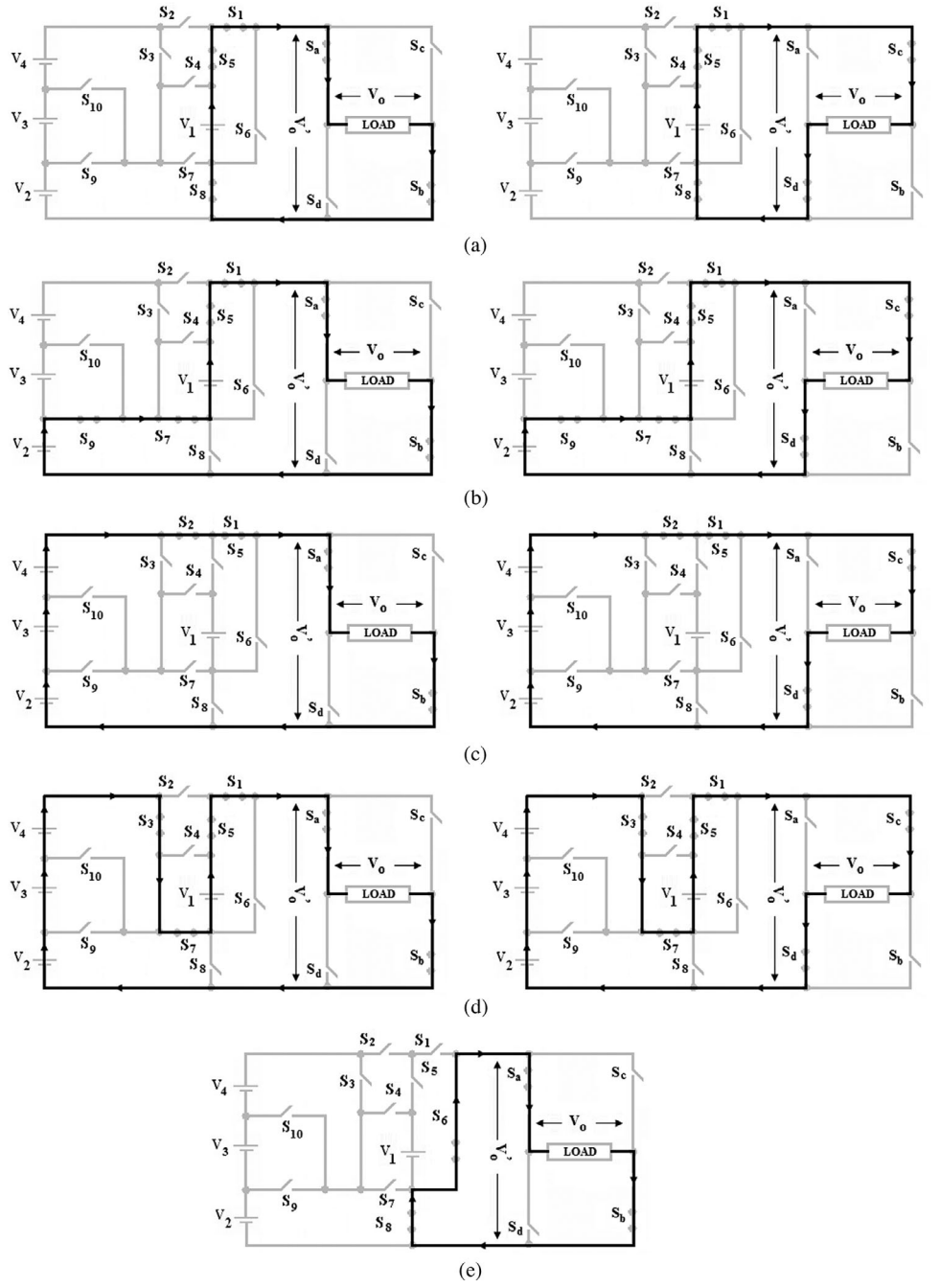


FIGURE 2 Equivalent circuit of nine-level inverter with various operating modes. (a) $\pm V_{IN\_1}$; (b) $\pm(V_{IN\_1}+V_{IN\_2})$; (c) $\pm(V_{IN\_1}+V_{IN\_2}+V_{IN\_3})$; (d) $\pm(V_{IN\_1}+V_{IN\_2}+V_{IN\_3}+V_{IN\_4})$; (e) zero level.

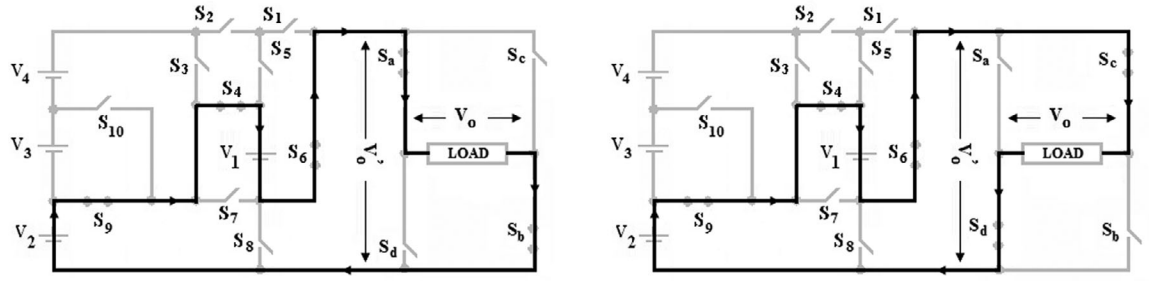


FIGURE 3 Modes of operation for asymmetrical inverter to attain $\pm(V_{IN\_2}-V_{IN\_1})$.

TABLE 1 Relationship between the proposed MLI with other similar MLIs proposed in the literature.

MLI topology	CHB	NPDC	FC	[25]	Proposed
Controlled switching devices	$2(s-1)$	$2(s-1)$	$2(s-1)$	$(3s-1)/2$	$(s+19)/2$
Diodes (bypass)	–	–	–	1	–
Diodes (clamping)	–	$2(s-3)$	–	–	–
Capacitors (DC-LINK)	–	$(s-1)/2$	$(s-1)/2$	–	–
Capacitors (clamping)	–	–	$(2s-6)/2$	–	–
DC input sources	$(s-1)/2$	1	1	$(s-1)/2$	$(s-1)/2$

TABLE 2 Generalized formula to extract various power components between the proposed MLI (n = 4 × k) and recent topologies.

Topology	N_{sw}	$N_{sw(ud)}$	$N_{sw(bd)}$	N_{dc}	$N_{current.sw}$	TSV	N_{Level}
[34]	(9 × k)	(6 × k)	(3 × k)	(4 × k)	(2 × k)	$(40 \times k)V_{dc}$	(16 × k)+1
[35]	(12 × k)	(8 × k)	(4 × k)	(4 × k)	(6 × k)	$(53 \times k)V_{dc}$	(8 × k)+1
[36]	(3 × k)+8	(3 × k)+8	–	(k+1)	(k+4)	$\left(\frac{1}{2k+1}\right)\sum_{i=0}^{k} V_i$	(4 × k)+3
[37]	(10 × k)	(10 × k)	–	(4 × k)	(5 × k)	$[2^{4k+2}\text{-}1]\ V_{dc}$	$16 \times 9^{(k-1)}+1$
Proposed	(14 × k)	(6 × k)	(8 × k)	(4 × k)	(4 × k)+2	$88 \times \sum_{i=1}^{k} 11^{(i-1)}V_{dc}$	$\left[20 \times \left(\sum_{i=1}^{k} 11^{i-1}\right)\right] + 1$

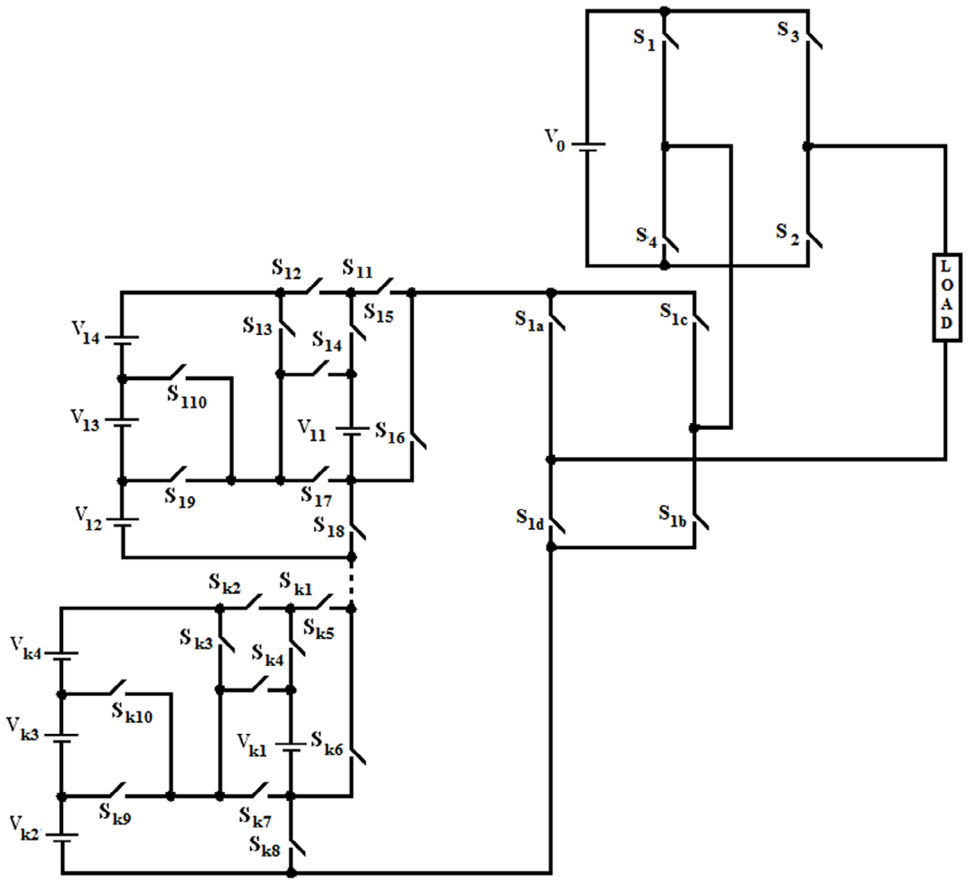


FIGURE 4 Hybrid topology.

TABLE 3 Comparisons of multilevel inverter symmetrical and asymmetrical configurations.

Parameters	Symmetrical	Asymmetrical (1:2)	Asymmetrical (1:3)
Maximum possible peak load voltage	$V_{dc}[(k \times 4)+1]$	$V_{dc}[(k \times 8)+1]$	$V_{dc}[(k \times 12)+1]$
Maximum possible voltage steps (or levels)	$[(k \times 8)+3]$	$[(k \times 16)+3]$	$[(k \times 24)+3]$
Total input DC voltage sources and capacitors	$[(k \times 4)+1]$	$[(k \times 4)+1]$	$[(k \times 4)+1]$
Total power devices	$(k \times 10)+8$	$(k \times 10)+8$	$(k \times 10)+8$
Proposed topology-total standing voltage (TSV)	$4V_{dc}$	$4V_{dc}$	$4V_{dc}$
H-bridge inverter			
Auxiliary module	$18 \times k \times V_{dc}$	$18 \times k \times V_{dc}$	$18 \times k \times V_{dc}$
Auxiliary H-bridge inverter	$16 \times k \times V_{dc}$	$16 \times k \times V_{dc}$	$16 \times k \times V_{dc}$

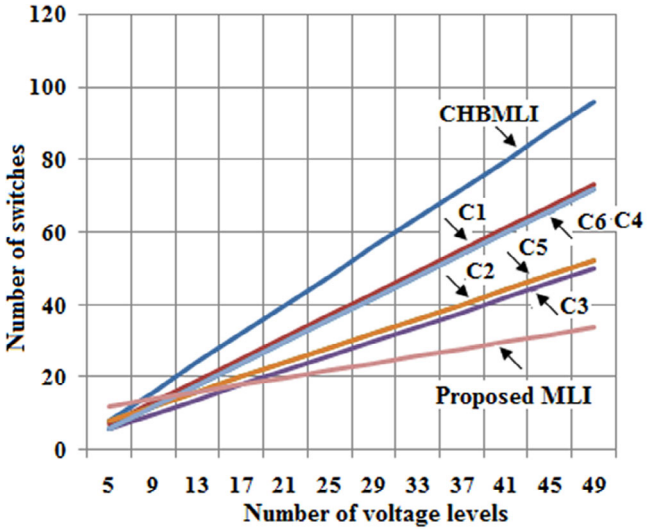


FIGURE 5 Multilevel inverters power devices vs voltage levels.

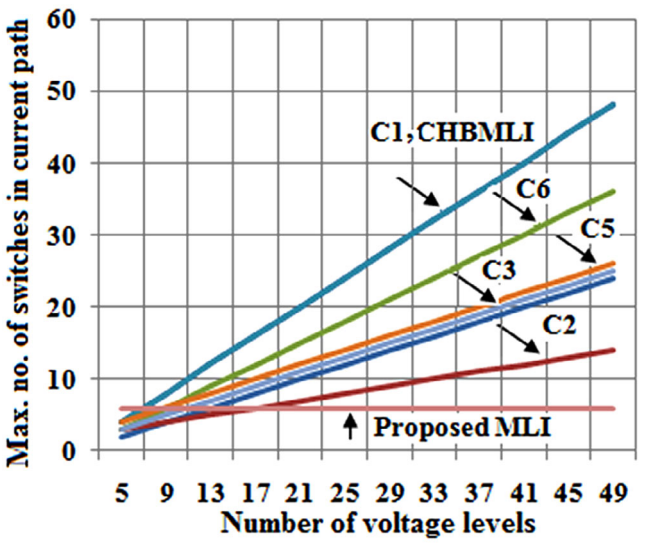


FIGURE 6 Variation of switching elements in current path with voltage levels.

higher voltage levels. If a proposed MLI structure is cascaded using four voltage sources with an H-bridge inverter and the voltage level of input DC power supplies is carefully chosen in the ratio of (1:2) and (1:3), then the proposed inverter produces 19 and 27 levels. The H-bridge inverter built with an MLI structure produces more voltage steps as compared with conventional MLIs by utilizing fewer power elements. The relation between 'n' and 'k' is tabulated in Table 3.

The switching devices requirements are understood with several steps in load voltage between the proposed and conventional topologies. Here, the conventional and recent topologies like CHBMLI and [11, 12, 18, 23–25] are referred in Figure 5. It is observed that the switching device required by the conceptualized MLI is less rather than the existing MLIs. Similarly, the MLIs cited in [26–30] require more switches but the projected topology produced output voltage with 27 levels by using 23 switching devices only. The conceptualized MLI is optimal for producing a high-level of inverter output voltage with fewer switching devices. Figure 6 depicts the effect of the recommended circuit design with optimized switching elements in the current conduction path with minimum power loss. Figure 7 depicts the structure of a three-phase power circuit for the projected MLI. The three-phase circuit requires one isolated DC voltage V_1 for each phase and the remaining voltage sources (V_2-V_n) are common to all phases. However, the projected topology needs one-third of DC voltage sources as compared with conventional cascaded MLI topology. Three numbers of single-phase HFT (high-frequency transformers) are needed to connect the three-phase load to the three-phase source. The HFT is connected either in delta or star depending on the load.

3 | OPTIMAL STUDY

By cascading the suggested topology as indicated in Figure 1 and the proper selection of voltage sources, the cascaded structure generates more voltage steps with minimal DC sources, gate driver units, and switching devices. Figure 1 depicts the optimized structure to produce higher voltage levels with the

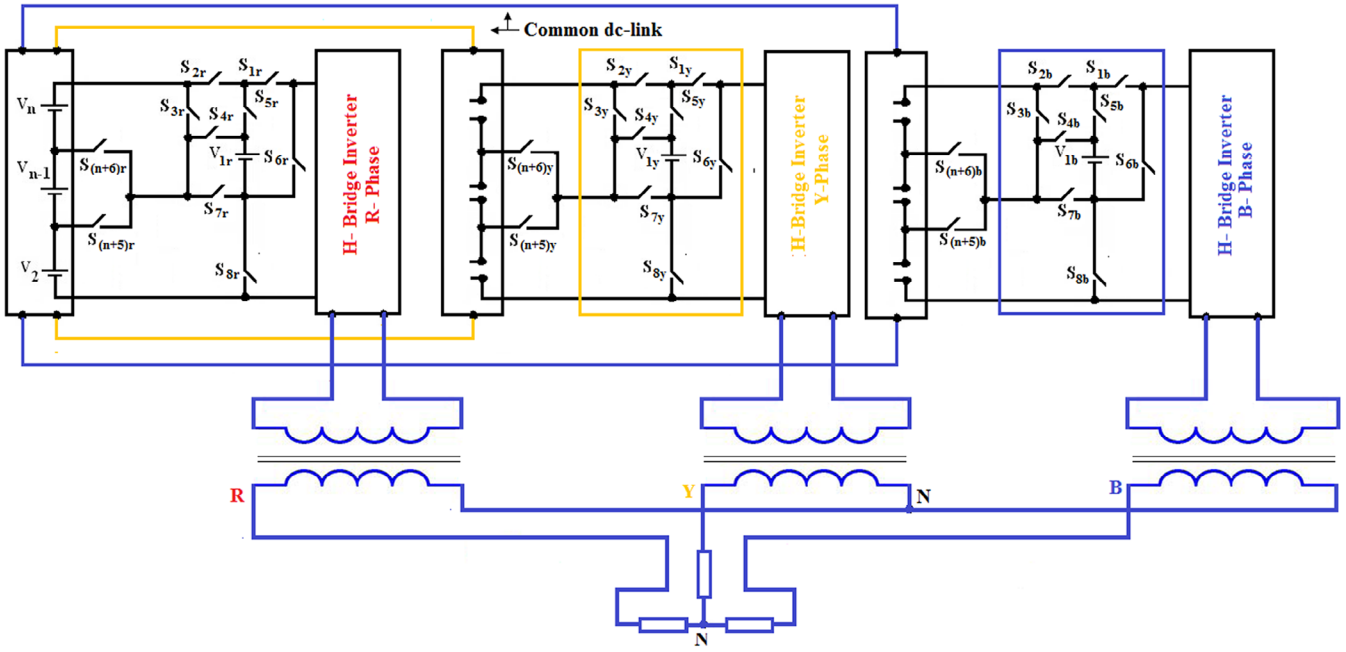


FIGURE 7 Proposed three-phase topology.

objective of a reduced power structure with low fabrication cost and reduced power components.

$$\text{No. of steps in load voltage} = ((n \times 2) + 1)), \tag{1}$$

$$\text{No. of switching devices} = (n + 10), \tag{2}$$

$$m = \prod_{i=1}^{k} ((2 \times n_i) + 1), \tag{3}$$

where 'n_i' and 'k' are the number of isolated DC input sources in each sub-MLC and sub-MLC topology.

No. of power devices in the suggested cascaded MLI structure is

$$S = (n_1 + n_2 + n_3 \ldots n_k) + 10k. \tag{4}$$

The proposed topology is optimized to produce more steps in the load voltage, constant switching devices, input sources, and associated gate drivers.

For this, consider Equations (1)–(4) and assume

$$\text{Isolated voltage sources in each MLI as } n_1 = n_2 = \cdots = n_k = n. \tag{5}$$

Using (1) and (5), the highest number of voltage levels could be achieved as

$$m = ((2 \times n) + 1))^k \tag{6}$$

Also using (4) and (5), the constant number of switching devices is obtained as

$$S = (n + 10) \times k, \tag{7}$$

$$m = [((nx2) + 1)]\ S/n + 10, \tag{8}$$

$$N_{Source} = \sum_{i=1}^{k} n_i = n_1 + n_2 + n_3 \ldots n_k. \tag{9}$$

Using (5), the no. of separated direct current sources may be expressed as

$$N_{Source} = n \times k. \tag{10}$$

Then the utmost no. of levels in load voltage can be determined

$$m = [((nx2) + 1)]\ N_{Source}/n \tag{11}$$

$$N_{Switch} = N_{driver} = \frac{(10 + n) \times \ln (m)}{\ln ((nx2) + 1)}. \tag{12}$$

Figure 8a predicts the variation of $((n \text{ x } 2) + 1)^{1/(n+10)}$ against 'n'. It is observed that more steps in load voltage are acquired for $n = 6$. Figure 8b confirms the variation of $((n \text{ x } 2) + 1)^{1/(n)}$ against 'n'. It is inferred from Figure 8b that a higher count of voltage steps is attained for $n = 3$. Figure 8c shows that the least value of switching devices to recognize 'm' values for the output voltage is promising at $n = 6$. While 'm' is kept constant, the total switching devices 'N_{Switch}' and 'N_{driver}' will be minimized, as soon as $(n+10)/\ln((2 \times n) + 1)$ are drawbacks likely to be minimum.

Figure 8d depicts the minimal gate drive circuits required to attain 'm' voltage steps in the load voltage for $n = 6$.

It is also necessary to compare the proposed topology in an asymmetrical configuration using the optimal structures design,

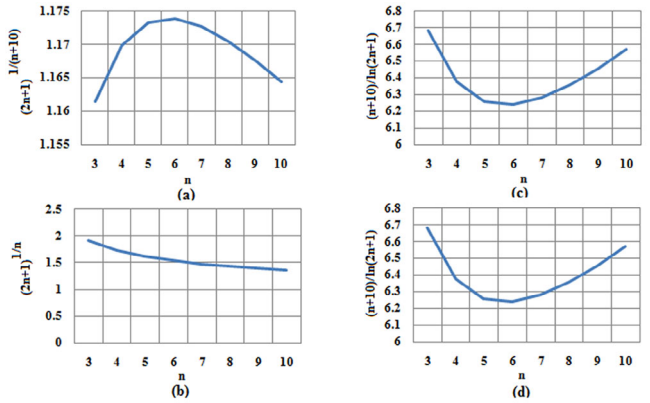


FIGURE 8 Graphical prediction to attain optimal structures using proposed topology.

maximum voltage steps were obtained with the minimum count of switching devices for $n = 6$. Using this constraint, the proposed topology is configured to operate with two MLI stages using $n = 6$ in each stage to produce stepped voltage with 32 switching devices. The measurement of the level of voltage sources is significant for effectively operating the MLIs in asymmetrical configurations to obtain high voltage levels. To realize the suggested topology in asymmetrical configuration and the design results obtained from power components optimization, the algorithms [P_1-P_9] reported in [18] are considered for comparative study. The projected topology using the algorithms [P_1-P_9] is suitably tailored to create voltage levels in both polarities. Using these procedures [P_1-P_9], the proposed topology offers 25, 45, 47, 49, 57, 79, 61, 73, and 177 levels in the output voltage using only 26 switching devices and the topology cited in [18] requires 36 switching devices for 12 voltage sources.

4 | ANALYSIS OF POWER LOSS

The outlined configuration is recommended for utility applications due to its good efficiency with less power loss as compared with conventional topologies. Therefore, it is mandatory to undergo power loss analysis in the MATLAB/SIMULINK platform by analytical expressions [32]. The switching and conduction loss can be envisaged from the operating curves of the semiconductor switches available in the datasheet. Here, power loss calculations have been introduced by considering both conduction and switching loss. The IGBTs (IRG4BC20SD) used in the experimental prototype have a maximum permissible conduction current of 19 A and 600 V with standing DC voltages.

The operating curves are (V_{sat} (θ) × I_L (θ)) and (E (θ) × I_L (θ)), where V_{sat} is the saturation voltage during the ON state of the device (collector to emitter voltage for the IGBT (V_{ce} (θ)) and forward voltage (V_F (θ))), and E (θ) is the energy lost in a single switching state (E_{ON} (θ) is a turn-on, E_{OFF} (θ) the turn-off conditions, and E_{rec} (θ) is indebted for the backward recovery process of the diode).

The graphs are estimated using Equation (13)–(21) by a curve analysis tool accessible in MATLAB.

The analytical equations are expressed for switching devices

$$V_{ce} = 9.6 \times e^{0.016} I_L(\theta) - 4.654 \times e^{-0.44} I_L(\theta), \quad (13)$$

$$V_F = 6 \times e^{0.02} I_L(\theta) - 4.258 \times e^{-0.275} I_L(\theta), \quad (14)$$

$$E_{rec} = 8.06 \times e^{-0.0322} I_L(\theta) - 0.57 e^{-0.446} I_L(\theta), \quad (15)$$

$$E_{ON} = 0.41 \times e^{0.44} I_L(\theta) - 0.37 \times e^{-0.8} I_L(\theta), \quad (16)$$

$$E_{OFF} = 4.43 \times e^{0.0021} I_L(\theta) - 5.47 \times e^{-0.107} I_L(\theta) \quad (17)$$

$$I_L(\theta) = I_m \sin(\theta - \varphi). \quad (18)$$

Here I_L (θ) denotes the output load current and φ denotes the phase angle of the load.

The switching-related power loss (P_{sw}) is calculated for each switching device during one switching period as given below:

$$P_{sw} = \frac{\sum (E_{OFF} + E_{ON} + E_{rec})}{T}. \quad (19)$$

When the switching device conducts, the conduction losses are calculated. It is calculated by taking the product of voltage during the process of turning ON (V_{CE} (θ)) and current during the process of turning on (I_l (θ)).

The conduction losses are evaluated as follows

$$P_{conT} = \frac{1}{2\pi} \int_0^{2\pi} V_{CE}(\theta) I_l(\theta) d\theta \quad (20)$$

$$P_{conD} = \frac{1}{2\pi} \int_0^{2\pi} V_F(\theta) I_l(\theta) d\theta \quad (21)$$

The power loss variations between the projected and conventional circuit designs are displayed in Figure 9. It has been

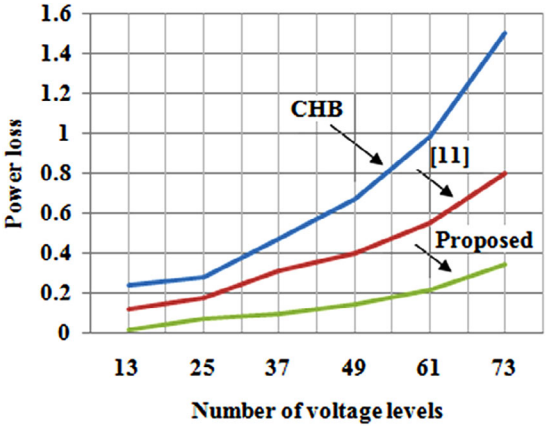


FIGURE 9 Multilevel inverter's power loss against voltage levels.

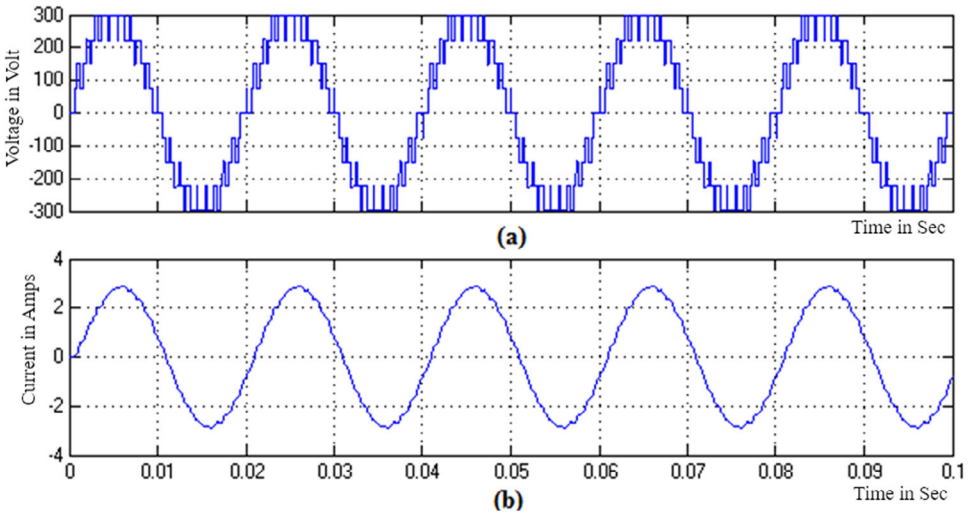


FIGURE 10 Nine-level inverter. (a) Output voltage and (b) inductive load current waveform.

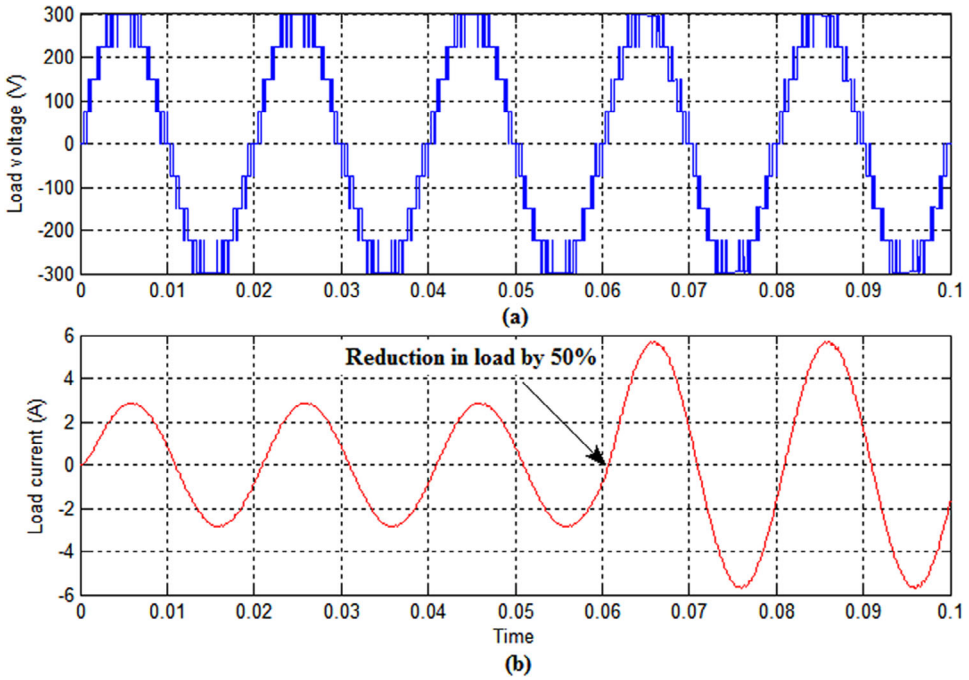


FIGURE 11 Nine-level inverter. (a) Output voltage and (b) inductive load current for change in load.

noticed that the recommended circuit design produces high level output voltage with minimum power loss.

5 | SIMULATION OUTCOMES AND ANALYSIS

The proficiency of the suggested topology with an RL load of 100 Ω and 100 mH has been verified through Matlab/Simulink for various values of input voltage sources. Multicarrier PWM strategy is taken for producing the PWM pulses for the switching devices to synthesize PWM modulated stepped voltage waveform with a switching frequency of 2 kHz and output frequency of 50 Hz on the load side. The proposed topology is a modular structure and the PWM generation is a crucial process in switching the power switches to get each level of the output voltage. The methodology involves base PWM generation and actual PWM required for each level. The base PWM is obtained by comparing triangle carrier and sine reference which are suitable logically XOR to get actual PWM for individual switches in the suggested topology. The analysis has two folds: symmetrical and hybrid topologies. The simulated response of symmetrical

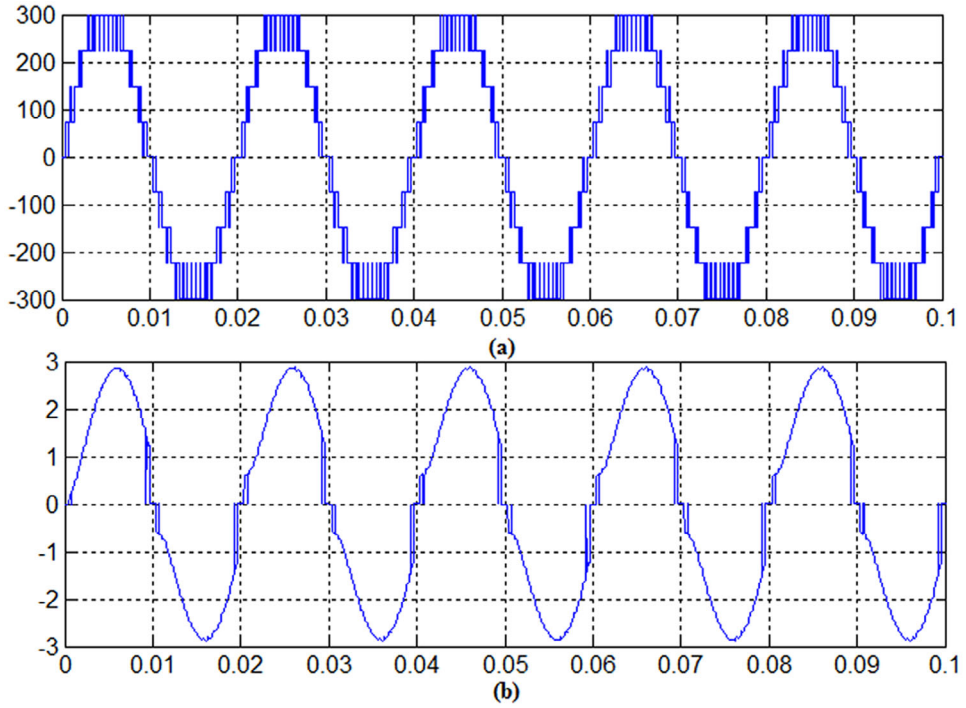


FIGURE 12 (a) Output voltage and (b) load current for nine-level inverter with non-linear load.

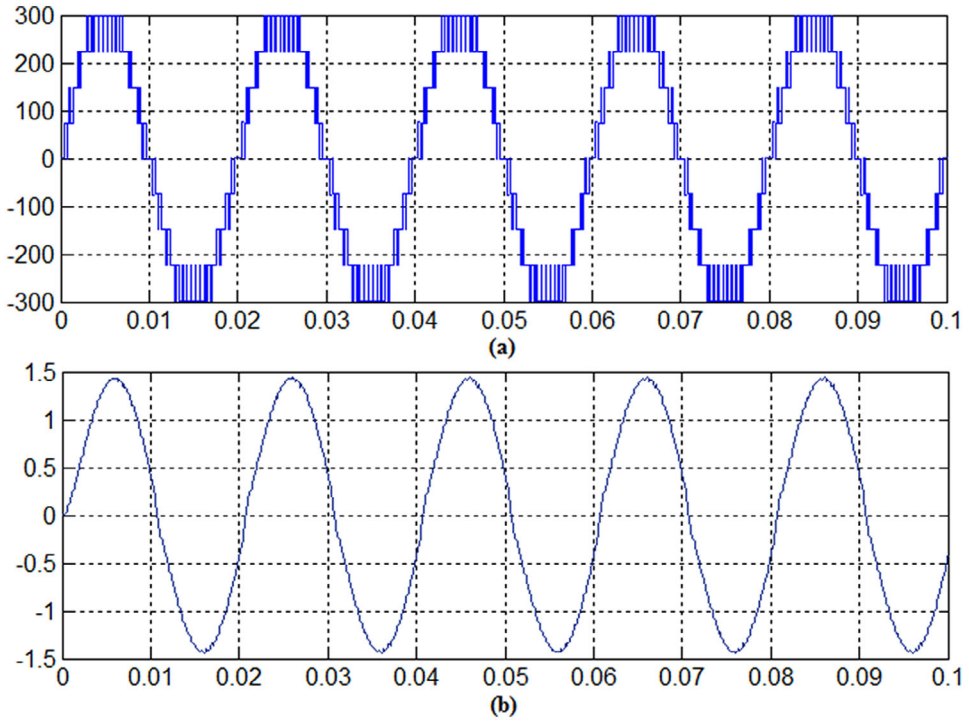


FIGURE 13 (a) Output voltage and (b) input current at the diode rectifier with L filter.

configuration for 9 levels is obtained with input voltage $V_1 = V_2 = V_3 = V_4 = 75$ V and to produce the peak output voltage of 300 V. Similarly for asymmetrical configuration with four voltage sources and a ratio of $[V_1: (V_2 = V_3 = V_4)] = (1:3)$ to result in a 21 step in the output voltage with $V_1 = 30$ V. For hybrid topology, the input parameters are $V_0 = 10$ V, $V_1 = 20$ V, and $V_2 = V_3 = V_4 = 40$ V to create the peak terminal voltage of 150 V, respectively. The simulated output voltage and current

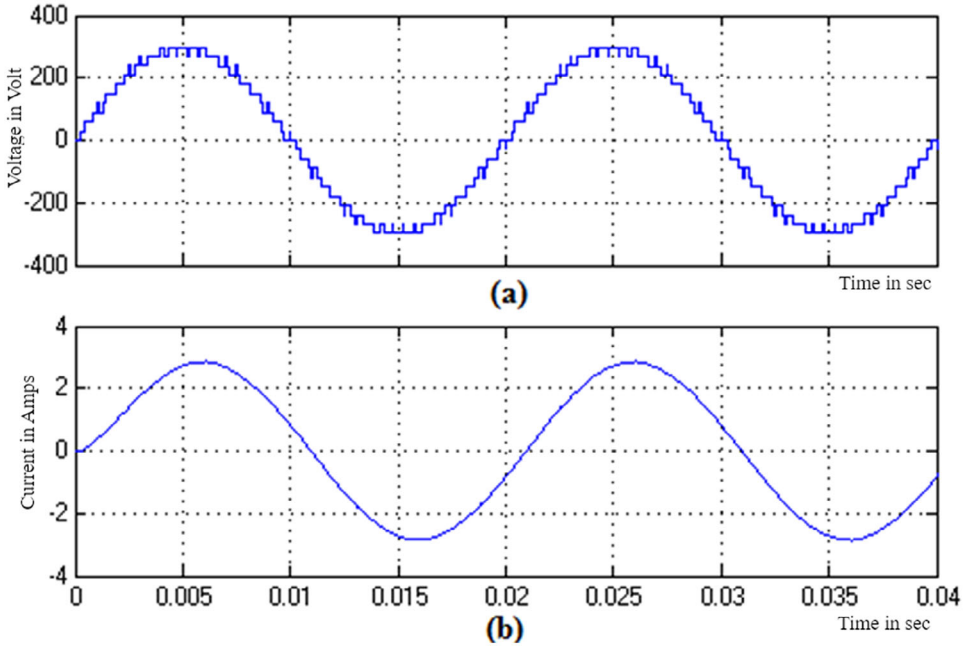


FIGURE 14 Twenty-one level inverter. (a) Output voltage and (b) inductive load current.

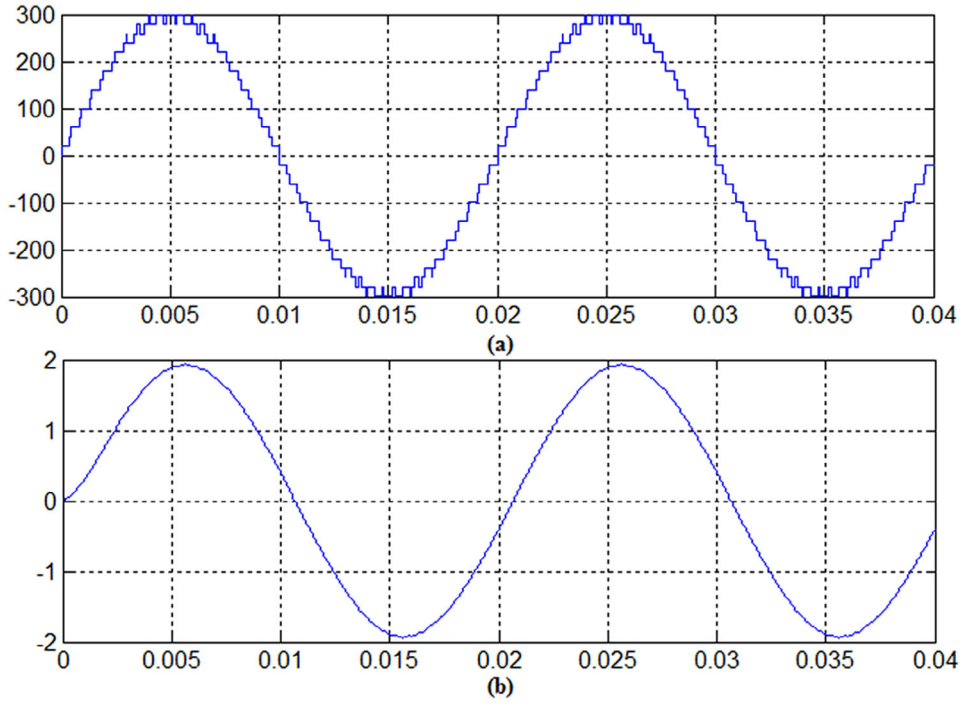


FIGURE 15 (a) Output voltage and (b) load current for 31-level inverter.

waveforms for the 9-level inverter are portrayed in Figure 10. The load is suddenly decreased to 50%, and the proposed topology responds well to the change with steady output voltage and a corresponding change in load current as shown in Figure 11. The proposed MLI is tested with non-linear load obtained by connecting a diode bridge in the load side of the MLI with an RL load of 100 Ω, 100 mH and the results are presented in Figure 12. It is observed that the proposed MLI responses well with non-linear load. It is seen that the quality of the output voltage remains unaffected and the shape of the output current in the MLI is non-linear. Due to this effect, there is an introduction of harmonics in the load current, and its THD for 9-level

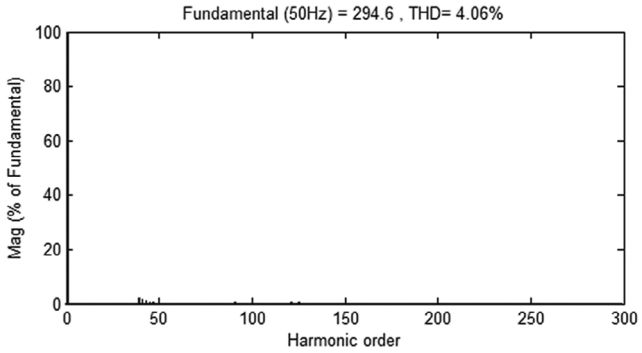


FIGURE 16 Output voltage spectrum for 31-level inverter.

TABLE 4 Analysis of simulation and experimental outcomes.

	Simulation		Experimental	
Proposed MLI	**Output voltage (V)**	**THD (%)**	**Output voltage (V)**	**THD (%)**
9-level	211.5	13.47	203.6	13.5
21-level	210.1	5.66	206.7	5.77
31-level	104.2	4.06	106.4	3.97

inverter for linear/non-linear load is obtained as around 5% and 12% with the same fundamental current of 2.8 A, respectively. To improve the quality of the MLI load-side current, an inductor filter of 100 mH is added at the input side of the diode bridge rectifier. This reduces the THD value to 5.96%, as shown in Figure 13. Similarly, the simulated output voltage and current waveforms for a 21-level inverter are portrayed in Figure 14. Figures 15 and 16 show the fundamental output voltage of 294.6 V (peak) and 209 V (rms) of a 31-level inverter with the same switching frequency of 2 kHz and modulation index of 1, resulting in the same THD value of 4.06%. Figure 17 shows the 31-level inverter simulation results, with an output voltage of 150 V (peak) and 104.2 V (rms), along with the current waveform for an inductive load as shown in Table 4. The simulation outcomes portrayed the potency of the recommended topology for asymmetrical voltage source ratios.

6 | EXPERIMENTAL OBSERVATIONS AND INTERPRETATION

The introduced topology has been experimented with the same specifications as those used in the simulation as seen in Figure 18. The introduced topology is constituted of various standalone power modules using IGBTs (IRG4BC20SD) and supporting driver circuits (IR2110). The main significance of the proposed topology is that it can be configured for the required level of output voltage with a minimum number of power modules and gate driver units. To operate the multilevel inverter, the essential firing pulses are generated using the Digilent Xilinx Spartan 3E-500 FG320 FPGA controller. The flow chart for FPGA-based PWM generation methodology is pictured in Figure 19. The flow chart generalizes the generation of firing pulses for the 'm' level inverter. The sine reference is regularly sampled and forms a look-up table. The sine data is retrieved from the stored memory address with the help of a counter support. Simultaneously, a step value is evaluated according to the carrier frequency to relate with the base value to produce a triangular carrier wave. Also, by comparing the carrier triangular wave and the reference sine wave, the PWM pulses are generated. The PWM pulses are tailored with the help of logical operators to generate the required pulses for the nine-level inverter. The same methodology is used to acquire the PWM pulses for the proposed asymmetrical configurations. The clock frequency of 50 MHz has been used for the pulse generation on-board. Modelsim simulation for reference and carrier generation along with base PWM pulses is displayed in Figures 20 and 21. The required FPGA program has been developed using VHDL coding and a bit file is created with the help of Xilinx-ISE software. By using Digilent Adept software, the bit file was

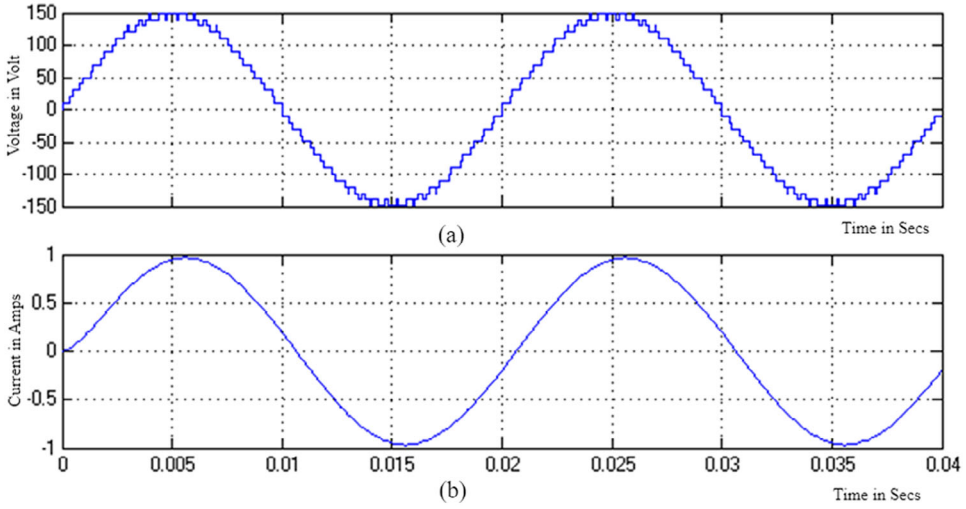


FIGURE 17 Thirty-one level inverter. (a) Output voltage and (b) inductive load current waveform.

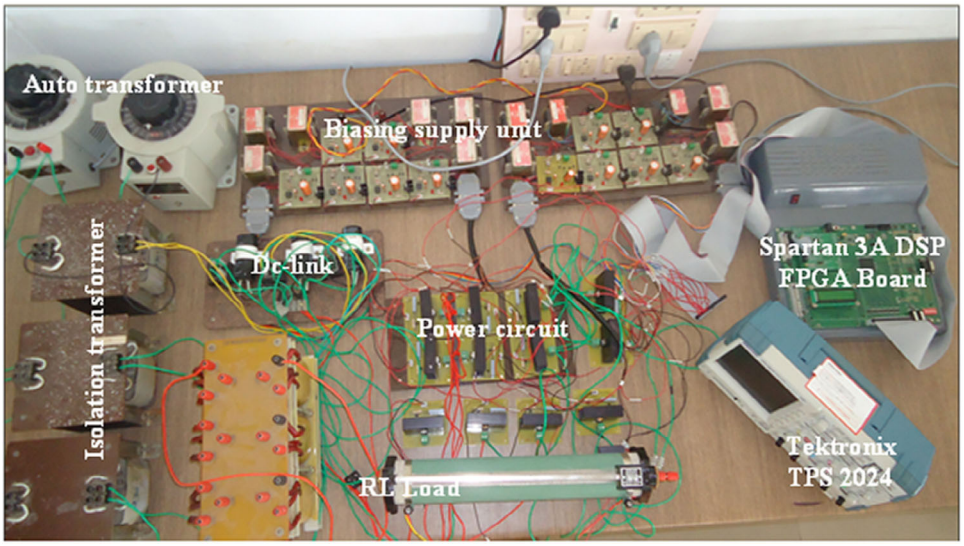


FIGURE 18 Experimental setup.

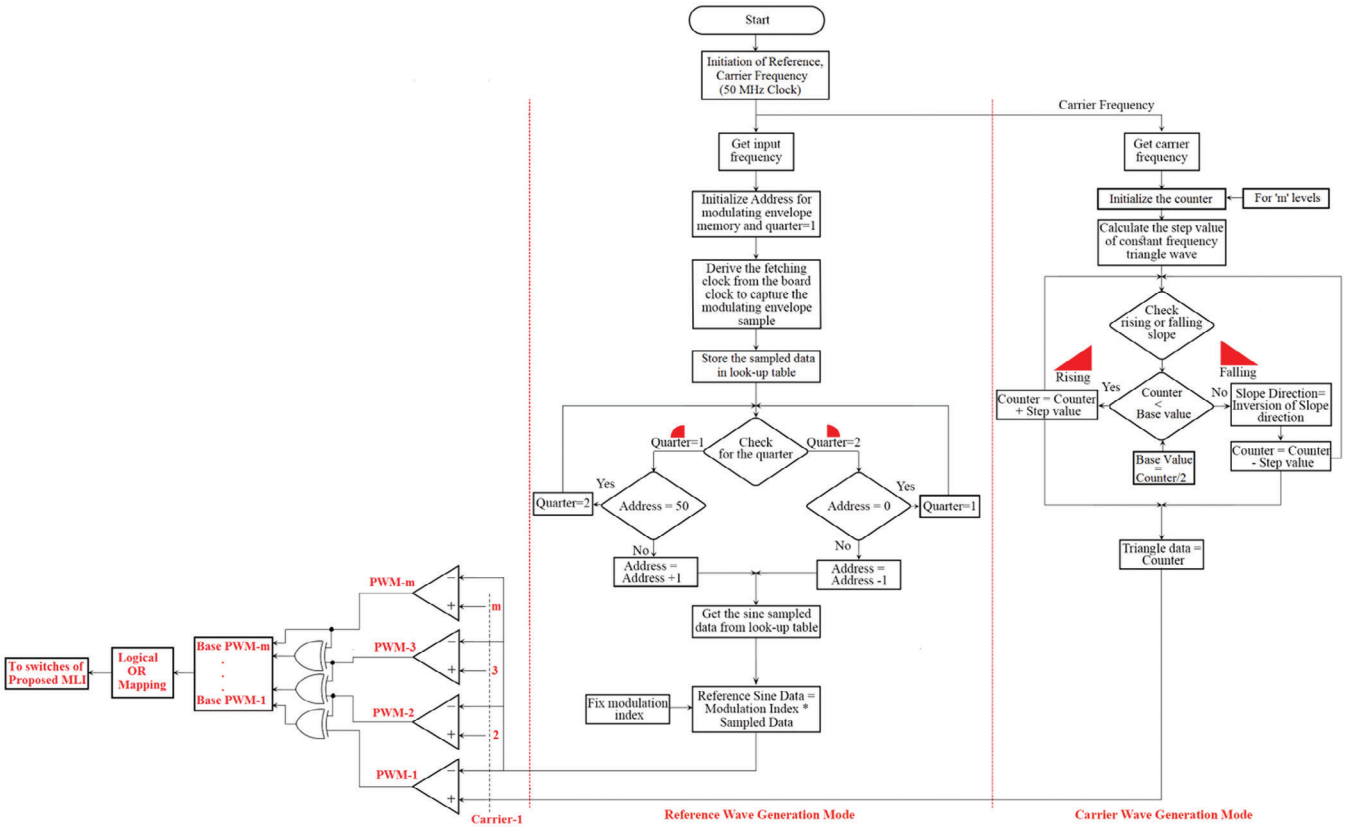


FIGURE 19 Flow chart for PWM generation using FPGA.

downloaded to the FPGA controller. The proposed topology operated in a symmetrical configuration to produce 9-level and the related outputs are illustrated in Figure 22. The dynamic load variation for 9-level inverter is portrayed in Figure 23 which authenticates the introduced MLI works well for such sudden variations. The proposed topology is configured in a hybrid configuration with one MLC cell containing three voltage sources and an H-bridge inverter resulting in a terminal voltage of 21-level. The corresponding output voltage along with inductive load current and voltage spectrum is represented in Figure 24.

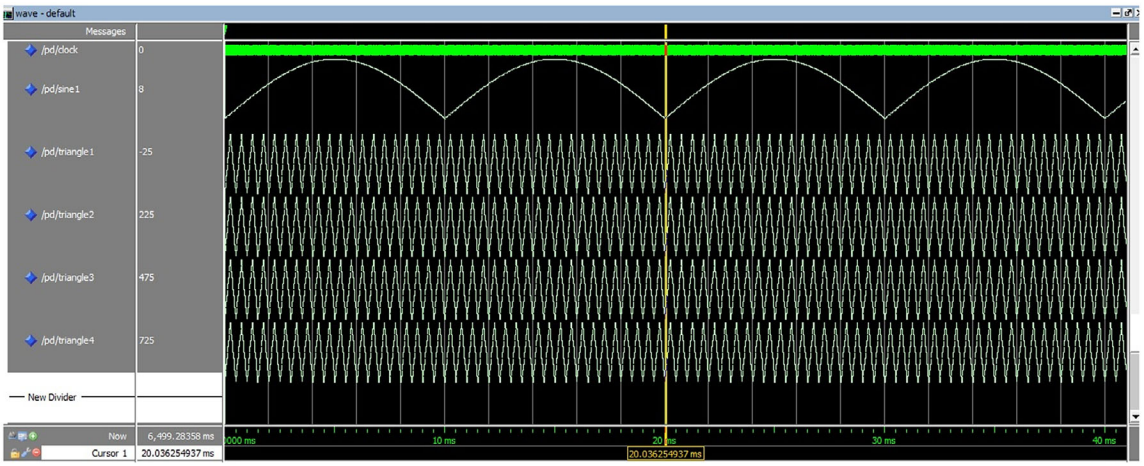


FIGURE 20 Modelsim simulation for reference and carrier signals.

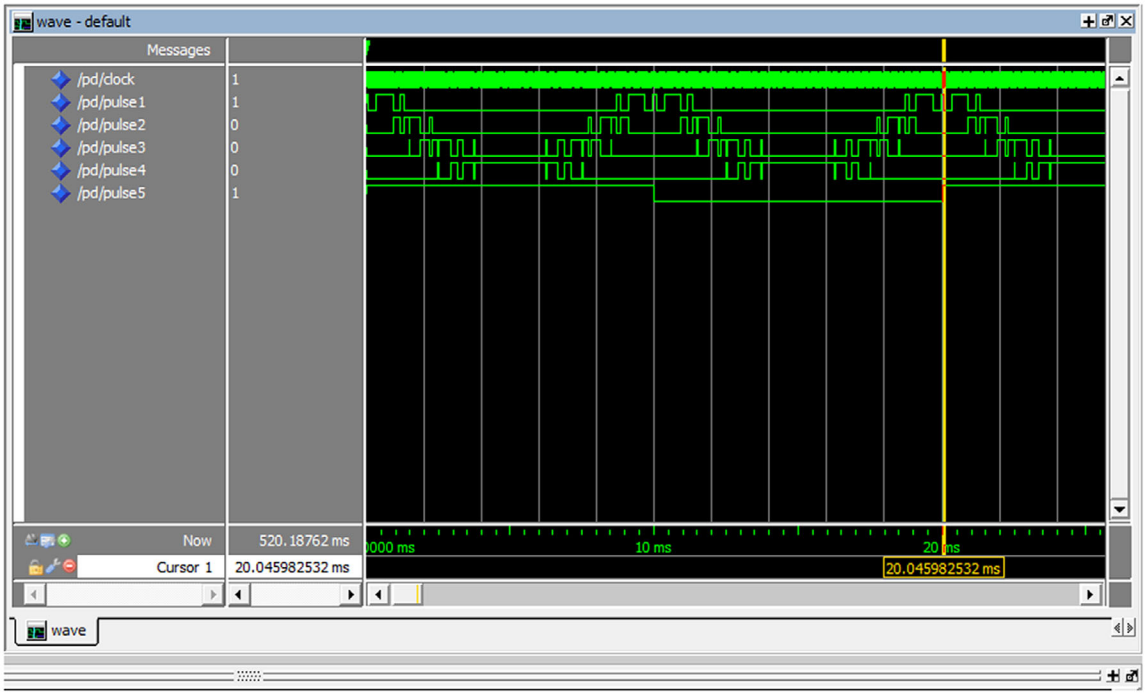
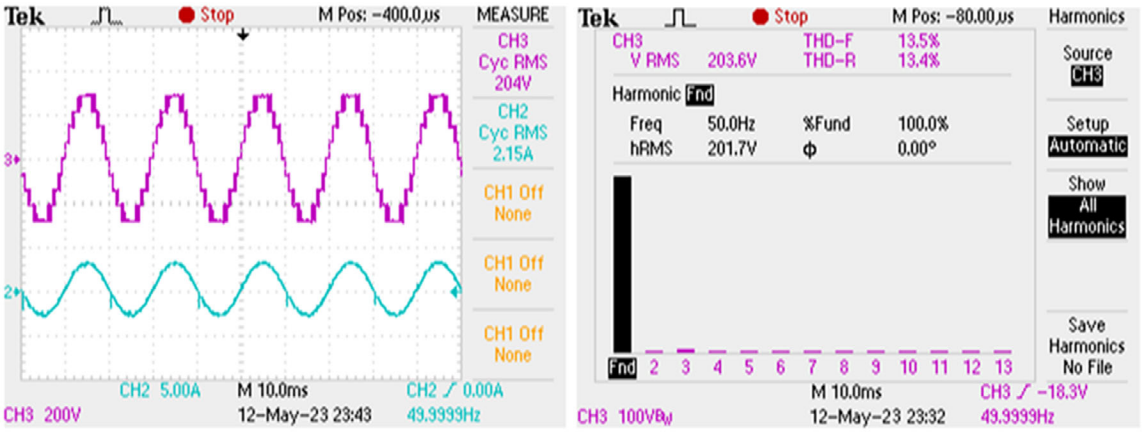


FIGURE 21 Modelsim simulation for base PWM pulses for 9-level inverter.



(a) (b)

FIGURE 22 Nine level inverter. (a) Output voltage and inductive load current. (b) Voltage spectrum.

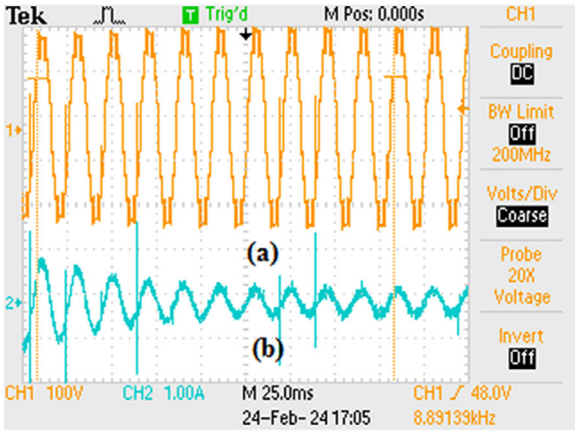


FIGURE 23 (a) Output voltage and (b) inductive load current waveform for dynamic load variations.

Also, Figure 25 depicts the results for a hybrid configuration combining one MLC cell with four voltage sources with an H-bridge inverter to produce 31 levels. The experimental results are portrayed by simulation outcomes. Table 4 compares the simulated response with laboratory prototype-based experimental results. The experimental value is slightly lower than the simulation due to the voltage drop across the switching devices.

7 | CONCLUSION

The proposed topology has been developed to claim the reduced number of DC sources, switches, and gate drivers to offer a higher number of voltage levels compared with classical topologies. Primarily, a sub-multilevel (MLC) module is developed to attain higher voltage levels with the minimum switching devices in the current conduction path to acclaim lesser power loss. Then a quad voltage source MLC cell is formed which originates from the proposed basic sub-MLC to further configure hybrid topologies for asymmetrical topologies. This topology projects its characteristics to add a few cells to produce higher voltage levels with binary and ternary voltage ratios. Based on the sub-MLC topology, optimal structures are arrived at with various constraints like the constant number of voltage sources, power semiconductor devices, and gate driver circuits for the constant number of voltage levels. The efficacy of the proposed

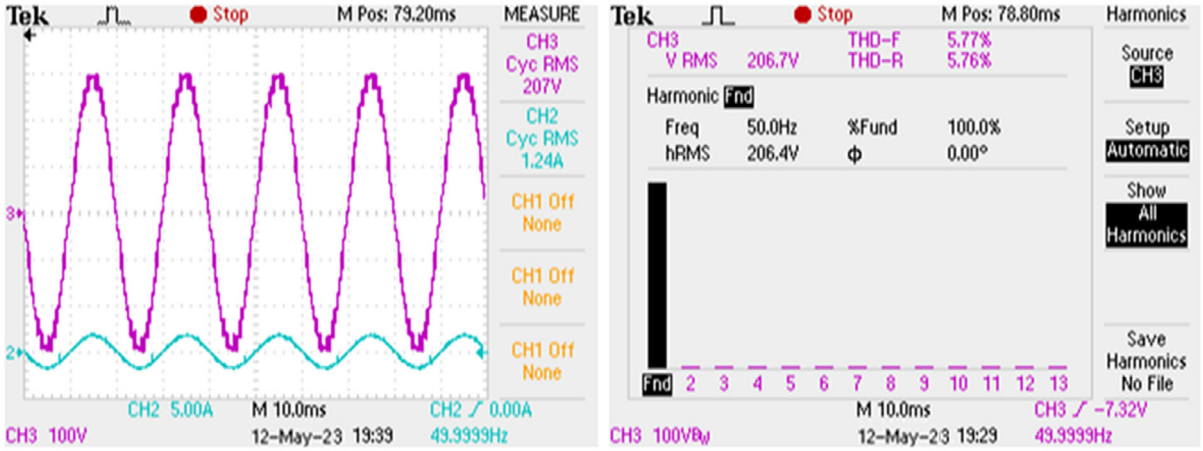


FIGURE 24 Twenty-one level inverter. (a) Output voltage and inductive load current. (b) Voltage spectrum.

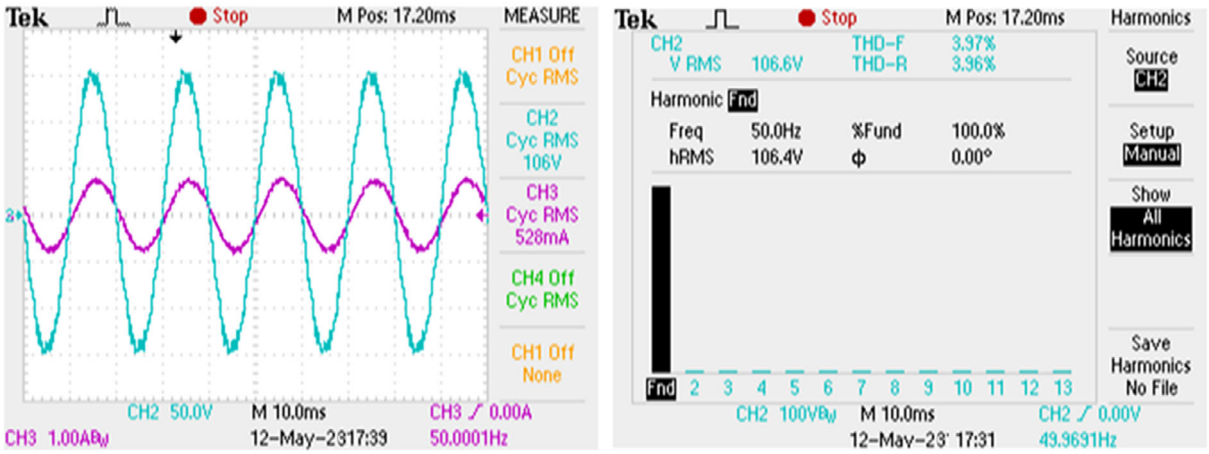


FIGURE 25 Thirty-one level inverter. (a) Output voltage and inductive load current. (b) Voltage spectrum.

topology has been verified through simulation and experimental setups, demonstrating high satisfaction and suitability for electric vehicle and renewable energy applications.

AUTHOR CONTRIBUTIONS

Ramesh Jayaraman: Conceptualization; data curation; formal analysis; investigation; methodology; software; validation; visualization; writing—original draft. **Sandirasegarane Thamizharasan**: Conceptualization; data curation; formal analysis; investigation; methodology; resources; software; validation; visualization; writing—original draft. **Jeevarathinam Baskaran**: Conceptualization; data curation; investigation; methodology; software; supervision; validation; visualization; writing—review & editing. **Veerpratap Meena**: Conceptualization; data curation; formal analysis; methodology; resources; software; validation; visualization; writing—review & editing. **Jitendra Bahadur**: Conceptualization; investigation; methodology; software; validation; visualization; writing—review & editing. **Vinay Kumar Jadoun**: Funding acquisition; investigation; resources; software; visualization; writing—review & editing.

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CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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