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Impact of Substrate Temperature on the Properties of Rare-Earth Cerium Oxide Thin Films and Electrical Performance of p-Si/n-CeO_2 Junction Diode

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Abstract
In this work, we report a p-Si/n-CeO_2 junction diode fabricated by a cost-effective and large-area deposition technique of jet nebulizer spray pyrolysis. The n-CeO_2 layer was coated on four different substrate temperatures (T_{sub}) 350, 400, 450, 500 °C and their properties were studied by various techniques like XRD, FE-SEM with EDX, UV–Vis and I–V characterization. XRD pattern confirmed a cubic fluorite crystalline phase of CeO_2 thin films with preferential growth along (2 0 0) direction. A smooth surface with inter-connected smaller grains was recorded by FE-SEM micrographs and also the existing elements Ce and O have been confirmed. For T_{sub} of 450 °C, an exceptional optical absorption with smaller band energy of 3.3 eV was recorded in the UV–Vis spectrum. The electrical conductivity results indicated that all the films are semiconducting in nature. I–V characteristics of all the fabricated diode showed better rectification in dark with excellent photovoltaic characteristics under light exposed condition. The photosensitvity of the diode varied from 21.94 to 1093.75% with substrate temperature. Our results strongly suggested that rare-earth based p-Si/n-CeO_2 diodes are suitable for future applications in ultraviolet photo-detector and photo-diode.

Keywords CeO_2 thin films · p–n junction diode · Spray pyrolysis · Photosensitivity · Photocurrent

1 Introduction

The p–n junction diode is a significant two layer semiconductor device and has pinched extensive attention for the past few decades due to its several promising properties like high forward current with low leakage current, superior rectifying behavior, switching property, etc. [1–4]. It has performed a major role in various electronic instruments including radios, computers, television and detectors. The performance of the diode can be improved by changing various external factors such as impurity distribution, biasing condition, device geometry and temperature [5, 6]. The junction diode can also detect light signals and effectively convert optical radiation into electrical energy. Recently, Cheng-Liang Hsu et al. investigated an ultraviolet/visible photo-detector based on p-NiO/n-ZnO junction and also analyzed its performance under various light sources [7]. The oxide materials having suitable bandgap with high electrical conductivity are the most promising candidate for fabricating good quality diode.

Cerium dioxide (CeO_2) is an interesting rare earth material and has played a curial role in various technological applications due to its excellent chemical stability, wide bandgap, high refractive index, optical transparency and dielectric properties [8–12]. The cubic fluorite crystal structure is one of the most commonly observed structure in CeO_2 thin films. In CeO_2 films, the Ce ions exhibit two different oxidation states like Ce^{3+} (trivalent) and Ce^{4+} (tetravalent) which are more adaptable for valency change switching development [13]. Typically, rare earth elements with good optical and luminescent properties will be highly suitable for optoelectronic applications like photo-diode, solar cell, photo-detector, etc. [14–16]. Especially, the cerium can exhibit superior photo-response in the visible region owing to their partially occupied 4f and 5d orbitals. It is noteworthy

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that the presence of nanostructured CeO_2 thin films with golf-ball like structure between the p-Si and Al interface effectively improved the photodiode properties of the MIS device [17].

Several works have been reported for the preparation of CeO_2 films like physical vapor deposition (sputtering, thermal evaporation, etc.) and chemical vapor deposition methods (sol–gel spin-coating, spray pyrolysis, etc.) [8–12]. Liu et al. [18] have fabricated a device using CeO_{2-x} nanocrystal thin film coated by magnetron sputtering method. Moreover, Foglietti et al. [19] have also fabricated heteroepitaxial structures consisting of epitaxial ceria film sandwiched between Pt upper electrode and a conducting substrate of Nb doped $SrTiO_3$. Acosta-Silva et al. [20] reported the sol–gel dip-coating method of preparing CeO_2 thin film and analyzed the impact of various annealing temperatures on the crystallite size and bandgap energy. Besides, Ramshanker et al. [21] studied the gas sensing properties of CeO_2 thin films deposited with different thicknesses by RF sputtering. However, it required a high operating power, vacuum during film deposition, long-time, large-space, high-cost, etc. Among these, jet nebulizer spray pyrolysis (JNSP) technique is a simple and inexpensive method which can offer a large area for coatings within a short-time [22]. It has high optical transmission, controllable film thickness and substrates with different shapes that can be deposited.

In this work, CeO_2 thin films were formed on the glass substrates at different temperatures of 350 °C, 400 °C, 450 °C and 500 °C by JNSP technique. The influence of substrate temperature on the CeO_3 thin film properties like structural, morphological, optical and electrical have been investigated. We have fabricated p-Si/n-CeO_2 junction diode using CeO_2 films as an n-type layer with high rectification factor. Both current–voltage (I–V) and current density–voltage (J–V) characteristics of the fabricated diodes were studied in dark and light exposed conditions. The impact of substrate temperature on p-Si/n-CeO_2 junction diode performance was examined based on reverse saturation current (I_o), ideality factor (n), and barrier height (Φ_B) parameters. Most importantly, the ON–OFF switching response of p-Si/n-CeO_2 diode was evaluated at variable time intervals.

2 Experimental Procedure

2.1 CeO_2 Thin Film Preparation

High purity cerium chloride (99.99%), quartz substrates and isopropyl alcohol were purchased from Sigma Aldrich. To prepare high-quality CeO_2 films, a 0.2 mol of cerium chloride was dissolved in 10 ml de-ionized water and stirred well (20 min) at room temperature by a magnetic stirrer. Before spray coating, each substrate was carefully cleaned with the soap solution and isopropyl alcohol to remove unnecessary impurities. The prepared solution was loaded in the solution reservoir and sprayed on the pre-cleaned substrates at various temperatures T_{sub} = 350 ºC, 400 ºC, 450 ºC and 500 ºC. Deposition parameters play a significant role in the film formation on the substrate, hence the pressure level and substrate size were fixed as 3.5 kg/cm^2 and 1.5 cm × 1.5 cm. Also, the diameter of the nozzle was maintained at 0.6 mm and the glass substrate is kept at 5–7 cm separated from the spray nozzle.

2.2 Fabrication of p-Si/n-CeO_2 Junction Diode

Boron doped p-type silicon wafers with (1 0 0) surface orientation was used for the fabrication of p-Si/n-CeO_2 junction diode. The purchased silicon wafers had 0–50 Ω cm surface resistivity and 250 µm thickness. Typically, the impurities like (dust, oil, grease, oxide layer, etc.) prevailing on the surface of wafers might affect the diode performance. Hence, all the wafers were carefully cleaned by adopting the following the procedure [23].

(I) Each Si wafer was degreased for 10–15 min in the boiling acetone and CH_3CH_2OH.
(II) The organic residues were removed from the substrates, through piranha solution by mixing of $H_2SO_4 + H_2O_2$ in the ratio of 3:1.
(III) Finally, the native oxide layer on the Si wafers were removed with the help of hydrofluoric (HF) acid diluted with H_2O in the ratio of 1:10.
(IV) Specifically, all the wafers were completely rinsed in deionized water after each step.

After the cleaning process, the prepared 5 ml solution was sprayed on the pre-cleaned silicon wafers (1 cm × 1 cm) at different substrate temperature T_{sub} = 350, 400, 450 and 500 ºC. As mentioned earlier the deposition parameters were maintained accordingly for the film formation. After CeO_2 layer coating, a silver paste was applied on either side of the fabricated diode for good electrical contact and it is dried for 6 h at room temperature.

2.3 Characterization Techniques

Crystallinity and structural parameters were analyzed by XRD (Rigaku Miniflex-II) with copper Cu Kα_1 radiation ($\lambda = 0.15406$ nm). Surface structure and elemental compositions were observed through FE-SEM (Zeiss Sigma). Optical absorbance and bandgap energy of the films were studied by UV–Vis spectroscopy (JASCO Model No. V-770PC). Film thickness was measured using stylus profile meter (Mitutoyo SJ 301). Electrical conductivity of the CeO_2 films and I–V characteristics of p-Si/n-CeO_2 diode were carried out using Keithley electrometer (Model No. 6517 B). The photocurrent variation of the diode was measured using portable solar simulator (PEC-L01).

3 Results and Discussion

3.1 XRD Analysis

Figure 1 portraits the XRD pattern of spray coated CeO_2 thin films deposited at various T_{sub} = 350, 400, 450 and 500 °C in which the primary peaks are observed at diffraction angle, 2θ (°) = 28.44 and 32.99 whose corresponding Miller indices are (1 1 1) and (2 0 0). When T_{sub} was increased from 400 to 500 °C, some of the additional peaks were revealed at 2θ (°) = 47.54, 56.54 and 69.42. The corresponding Miller indices are (2 2 0), (3 1 1) and (4 0 0) which is in good accordance with JCPDS Data No. 34-0394 [24]. All the coated CeO_2 thin films revealed a single phase polycrystalline nature consisting of cubic fluorite crystal phase. No phase change was observed in the films with higher T_{sub}. Interestingly, all the diffraction peaks were found to increase gradually along with substrate temperature. It is evident from XRD Pattern, that higher T_{sub} exhibit a better crystallinity when compared to lower temperature as seen in Fig. 1. The most preferential growth was observed along the (2 0 0) direction. Besides, the (1 1 1) plane seems to improve linearly up to 450 °C and then decrease slightly at 500 °C. This result suggests that a small variation in the substrate temperature has largely affected/improved the growth of CeO_2 films especially at 450 °C. The crystalline size of the film was calculated using Debye–Scherrer equation [24].

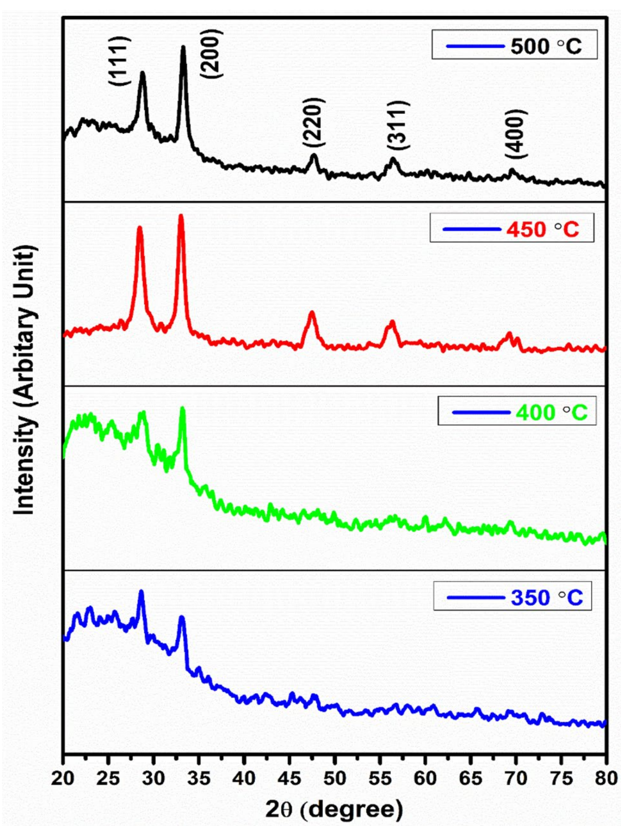


Fig. 1 XRD pattern of pure CeO_2 at various temperature

$$D = \frac{0.89\lambda}{\beta\cos\theta}, \tag{1}$$

where D is crystallite size, λ is wavelength (λ = 0.15418 nm), β is full width at half maximum diffraction of the peak and θ is the angle of diffraction. The average crystallite sizes (D) of the CeO_2 films were found to vary from 9.7 to 17.4 nm with different T_{sub}. The improvement in (D) of CeO_2 films with substrate temperature (up to 400 °C) is ascribed to coalesces of smaller grains into large size and reduction in the density of low angle grain boundaries [25, 26]. Interestingly, the CeO_2 films deposited at T_{sub} = 450 °C recorded the minimum average crystallite size (D = 9.7 nm). The micro-structural parameters such as micro-strain (ε), dislocation density (δ) and stacking fault (SF) of the CeO_2 films were calculated and summarized in Table 1 using the following formulae [24, 26].

$$\delta = \frac{1}{D^2}, \tag{2}$$

$$\epsilon = \frac{\lambda}{D\sin\theta} - \frac{\beta}{\tan\theta}, \tag{3}$$

$$SF = \left[\frac{2\pi^2}{45(3\tan\theta)^{\frac{1}{2}}}\right]\beta. \tag{4}$$

Figure 2 shows the variations in micro-structural parameters (ε, δ and SF) of the CeO_2 thin films deposited at various T_{sub}. From the Table 1, the average micro-strain (ε) and dislocation density (δ) of the films were found to vary between 2.07–3.89 × 10^{-3} and 0.37–1.37 × 10^{-16} lines/m^2 with substrate temperature. It was observed from Fig. 2 that the mean value of ε and δ decreases with increase in T_{sub} up to 400 °C. This might be associated with the reduced lattice imperfection and improved crystallinity of the films [27]. Thus, XRD results clearly indicated that the variations in substrate temperature can strongly improve the crystallinity of the film especially at T_{sub} = 400 °C.

Table 1 Structural parameters of CeO_2 thin films for various substrate temperature

Substrate temperature	2θ (°)	d (Å)	FWHM (Rads)	hkl	D (nm)	ε (× 10^{-3})	δ (× 10^{16} lines/m^2)	SF (× 10^{-2})
350	28.46	3.1355	0.0206	111	6.9	0.4993	2.0723	1.1528
	33.14	2.7026	0.0103	200	14.0	2.4690	0.5065	0.6326
400	28.84	3.0947	0.0103	111	13.9	2.4948	0.5172	0.5810
	33.27	2.6922	0.0068	200	21.0	1.6454	0.2249	0.4227
450	28.44	3.1381	0.0120	111	11.9	2.9132	0.7052	0.6721
	32.99	2.7146	0.0103	200	14.0	2.4699	0.5069	0.6307
	47.54	1.9123	0.0171	220	8.8	3.9290	1.2827	0.1364
	56.54	1.6275	0.0206	311	7.6	4.5374	1.7108	0.1926
	69.42	1.3537	0.0274	400	6.1	5.6467	2.6495	0.3407
500	28.82	3.0967	0.0120	111	11.9	2.9107	0.7040	0.6775
	33.31	2.6894	0.0060	200	24.0	1.4396	0.1722	0.3701
	47.62	1.9093	0.0103	220	14.7	2.3567	0.4615	0.8195
	56.61	1.6258	0.0137	311	11.4	3.0240	0.7598	1.2856
	69.75	1.3482	0.0274	400	6.1	5.6357	2.6392	3.4367

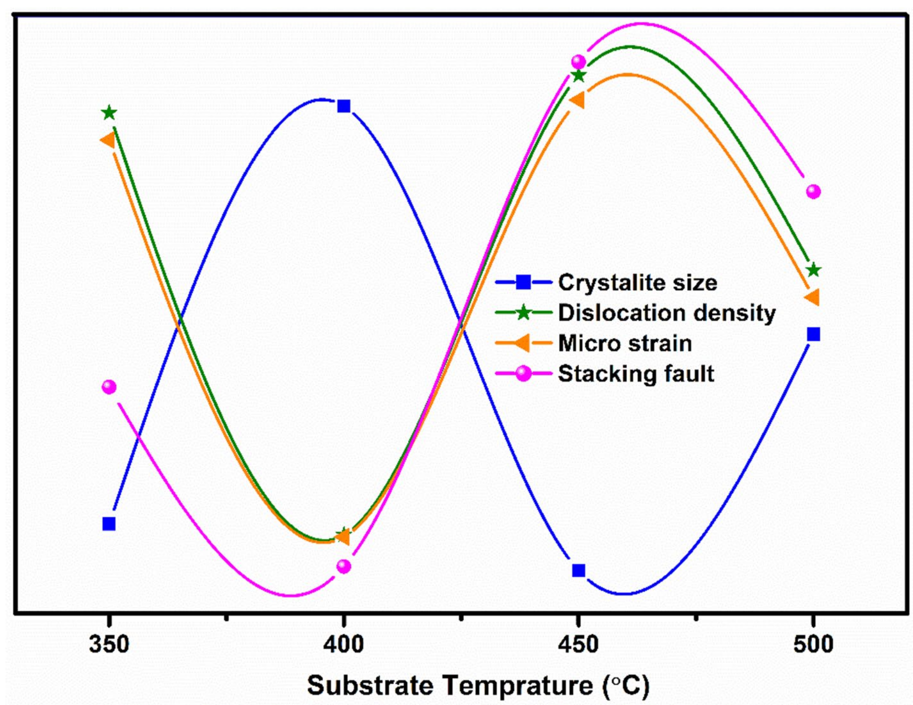


Fig. 2 Variation of structural parameters of CeO_2 films at different T_{sub}

3.2 FE-SEM and EDX Analysis

Surface structure and grain arrangement of the prepared CeO_2 thin films were analyzed through FE-SEM spectrograph. Figure 3 displays the FE-SEM images of spray deposited CeO_2 films at various substrate temperatures. All the films exhibited uniform surface with visibly interconnected grains. This outcome implies that our JNSP technique is highly appropriate for preparing films with smooth surface. The observed grain size varied approximately in the range of 10–50 nm (Fig. 3). No cracks were observed on the surface of the CeO_2 film even at higher T_{sub}. The CeO_2 films prepare with T_{sub} 400 and 500 °C showed better grain growth than other films. However, the grain growth was found suppressed at 450 °C. Grain size variation is in good accordance with mean crystallite of the CeO_2 films (Fig. 2). Smooth surface in the films can improve its electrical behaviour which can enhance the diode parameters and their performance [28]. Generally, thermal treatment strongly influences the crystallization growth process and as a consequence the surface

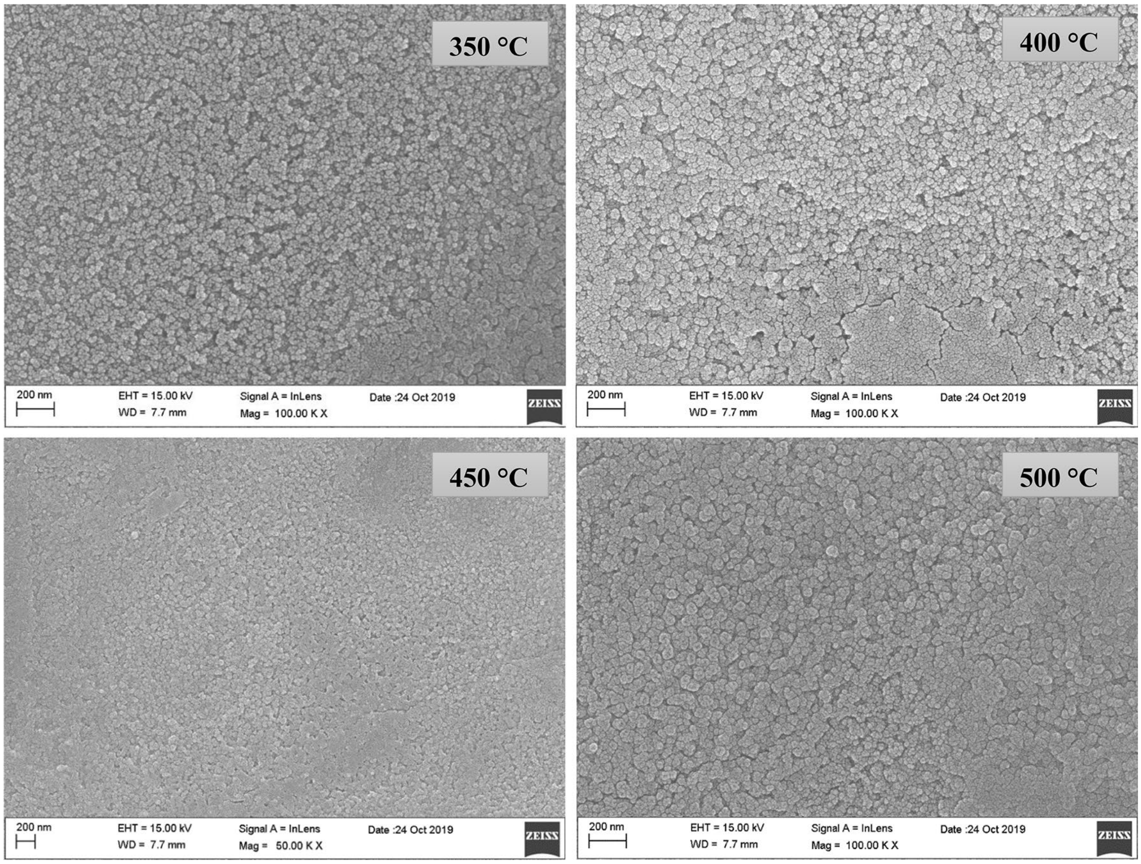


Fig. 3 FE-SEM images of spray deposited CeO_2 films at various substrate temperature

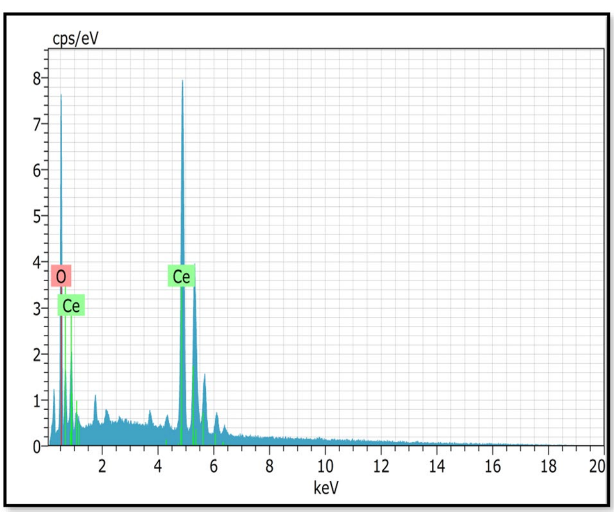


Fig. 4 EDX spectrum of spray deposited CeO_2 films at $T_{sub} = 450$ °C

morphologies and crystal structures are greatly affected. EDX spectrum of the CeO_2 thin film is shown in Fig. 4. The presence of elements like Ce and O were confirmed with the at.% of 31.46 and 68.54 respectively. The spray coated CeO_2 films has better stoichiometry property.

3.3 UV–Visible Spectroscopy

The absorbance spectrum of the CeO_2 films deposited on glass substrates at various substrate temperature is shown in Fig. 5. They expose a well-defined sharp and strong absorbance peaks between the wavelength range of 250 and 285 nm. The optical absorbance of all the films were found to increase up to 285 nm (i.e. UV region) and then reduced slowly till 400 nm. At higher wavelength (i.e. visible region), the absorbance values are almost constant. Compared to other T_{sub} the CeO_2 film formed at 450 °C recorded a maximum absorbance in both UV–Vis and visible region. This could be due to the formation of oxygen vacancy, coloration, film thickness and grain boundary of the CeO_2 film. The CeO_2 film with higher absorbance is highly appropriate for photovoltaic application [17–19, 24]. Moreover, a strong absorbance peak was observed at 276 nm for the film with $T_{sub} = 450$ °C which is relatively higher than other films. The shift in the absorbance peak toward longer wavelength is due to the blue emission. The optical bandgap

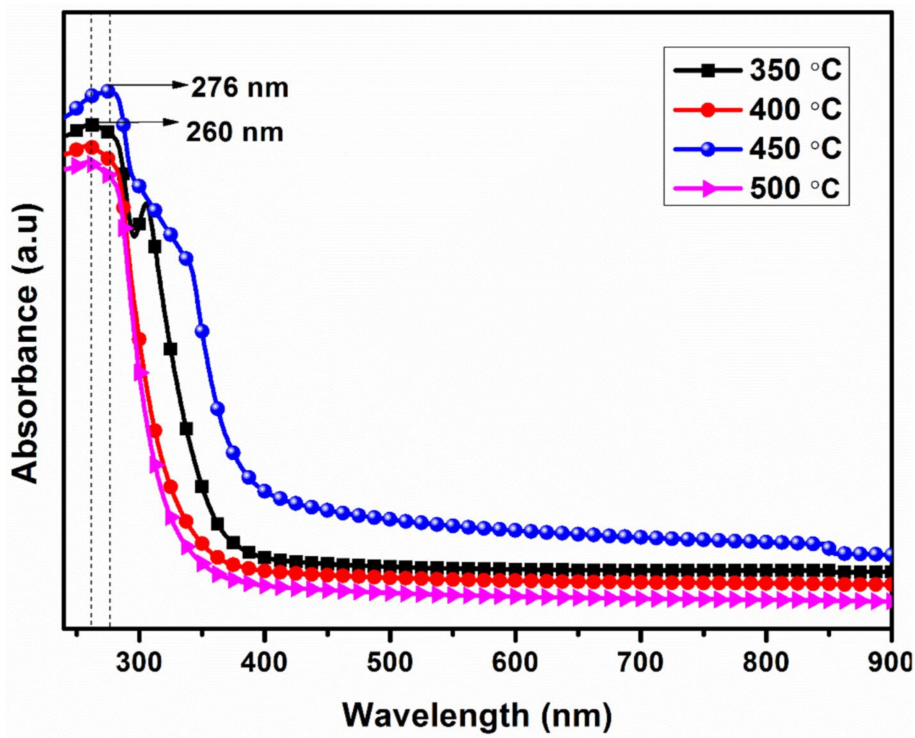


Fig. 5 Absorbance spectrum of pure and CeO_2 thin at various T_{sub}

(E_g) of the prepared thin film was calculated using the following the equation,

$$(\alpha h\nu)^2 = A(h\nu - E_g), \tag{5}$$

where α is the absorption coefficient, h is the Planck's constant, v is the photon energy, A is the constant and E_g is the band gap.

From Fig. 6, the calculated optical bandgap energy values were found to vary from 3.30 to 4.08 eV which was in

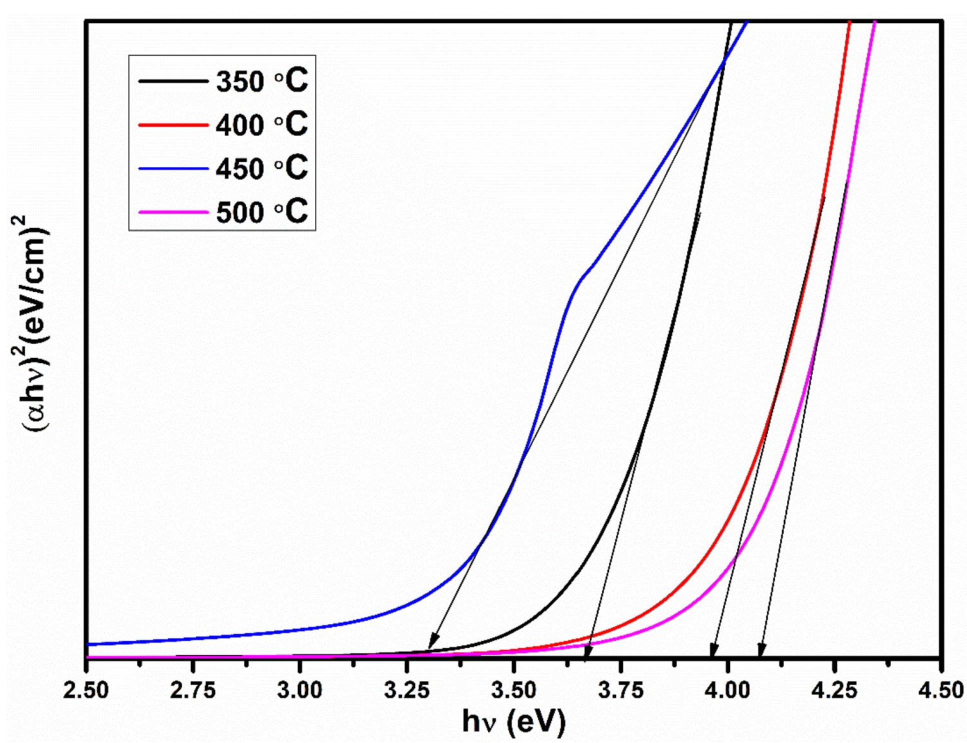


Fig. 6 Plots of $(\alpha h\nu)^2$vs.$h\nu$ for pure CeO_2 films at various T_{sub}

good agreement with earlier reports [8–11]. Notably, the minimum band gap ($E_g = 3.30$) energy was obtained at T_s of 450 °C. In fact the film with lower band gap energy might improve the charge transport properties of the electrical device. The increase in optical band gap energy is due to Burstein–Moss effect [29]. To further explore the optical properties of the deposited CeO_2 films we have calculated both absorption coefficient (α) and extension coefficient (k) using the following formula [30].

$$\alpha = \frac{\ln\left(\frac{1}{T}\right)}{t}, \tag{6}$$

$$k = \frac{\alpha\lambda}{4\pi}, \tag{7}$$

where α is the absorption coefficient, t is the thickness of the film, T is the transmittance, c is the velocity and λ is the wavelength of light.

The obtained α and k values are tabulated in Table 2 and these values are well matched with reported literature [30]. It is surprising that the CeO_2 film deposited at 450 °C attained higher absorption coefficient $\alpha = 492 \times 10^7\ cm^{-1}$ and extension coefficient ($k = 0.215$) when compared with the other films. The variation in the extinction coefficient of the CeO_2 film is directly related to the absorption of light. Moreover, the thickness of the CeO_2 films were analyzed at different substrate temperature. The increase in T_{sub} reduced the CeO_2 film thickness. This trend is analogous with the previously reported work by Acosta Silva et al. [20]. The measured film thickness are found to vary from 545 to 394 nm which is shown in Table 2. This variation is strongly influenced by the substrate temperature at which the film is synthesized. The atoms in the films are held together by certain adhesion energy and bind with each other for a given thickness. But as the substrate temperature increases, the thermal energy supplied overcomes the bond energy. Hence, atoms at the surface are desorbed leading to the reduced film thickness at higher T_{sub}. From the UV–Vis analysis of spray coated CeO_2 films, the optical parameters were found to vary with substrate temperature.

3.4 Photoluminescence

The variations in PL intensity and band emission with substrate temperature have been analyzed in the wavelength range 250–500 nm. Figure 7 depicts the PL spectrum of CeO_2 thin film coated at different T_s = 350–500 °C. It is obviously clear that all the films exhibited a broad-band character within the wavelength of 250–375 nm which signifies the presence of oxygen vacancy defect in CeO_2 films with electronic energy levels below 4f band [31]. In UV region, the CeO_2 film coated at T_{sub} = 450 °C recorded a strong emission peak with maximum intensity of 301.5 nm. The broad emission peak suggests that the electrons which are captivated in defect level are transmitted to O 2p level. Other films showed an emission peak at 298 nm with less intensity. Besides, the emission peak at 468 nm in the visible region implies the blue and green emissions. These emissions might be ascribed to the persistence of electron–phonon interaction within the Ce 4f and O 2p band [24]. The PL intensity of the CeO_2 films effectively changed with substrate temperature. On increasing substrate temperature (350–500 °C), the PL intensity increased steadily up to 450 °C and then reduced at higher concentration of 500 °C due the recombination of charge carriers (electrons–holes). It is observed from PL spectrum that the substrate temperature significantly modified the emission peaks of the CeO_2 films.

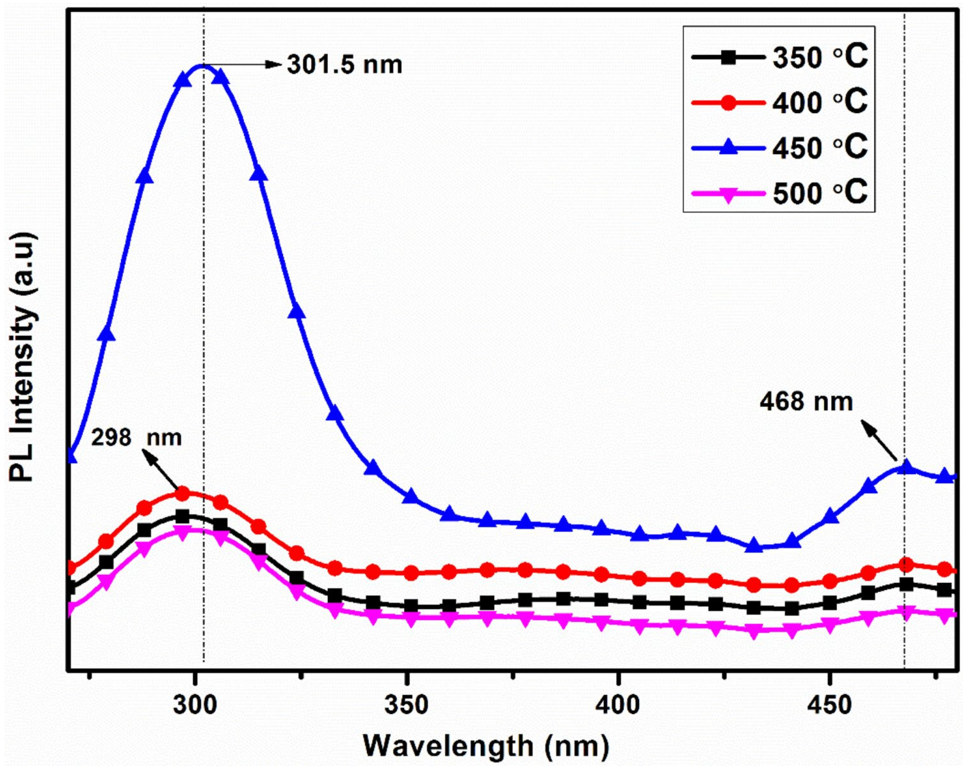
3.5 Electrical Conductivity

Controlling electrical the parameters of thin film is very much essential for the development of electrical devices such p–n junction diodes. Electrical resistivity, activation energy and conductivity of the CeO_2 films were evaluated by I–V characteristics using the two probe setup. Current values of the CeO_2 films were measured as a function of temperature ranging from 30 to 130 °C (step of 20) which is shown in Fig. 8. As predicted for all the temperatures, the current value increased linearly satisfying the ohms law. These values advocate the strong affinity of CeO_2 films on the measuring temperature and we have recorded the highest current value at 130 °C. The electrical resistivity can be determined by the following equation [26].

Table 2 Optical parameters of CeO_2 thin films for various substrate temperature

Substrate temperature (°C)	Absorption coefficient (α) $\times 10^7$ (cm^{-1})	Extension coefficient (k)	Band gap, E_g (eV)	Film thickness (nm) (∓ 5 nm)
350	0.138	0.060	3.66	545
400	0.119	0.052	3.96	487
450	0.492	0.215	3.30	428
500	0.121	0.053	4.08	394

Fig. 7 PL spectrum of CeO_2 thin films deposited at various T_{sub}



$$\text{Resistivity}\,(\rho) = \mathrm{R}\left(\frac{\mathrm{A}}{\mathrm{t}}\right)\Omega\mathrm{cm}, \tag{8}$$

where R is the resistance, t is the thickness and A is the area of the films.

The CeO_2 films coated at T_{sub} = 350 °C showed a resistivity of 1.46×10^9 Ω cm, which gradually reduced up to 450 °C and then increased marginally for 500 °C owing to the oxygen vacancy in the films. Decrease in CeO_2 film resistivity with substrate temperature is mainly attributed to the increment of the carrier concentration and carrier mobility which showed good agreement with Wang et al. [32]. The reduced grain boundaries and crystal lattice deficiency of the CeO_2 films with T_{sub} might have improved the mobility of the carriers, facilitating smaller resistivity in the films [33]. The electrical conductivity of the CeO_2 films have been calculated and tabulated in Table 3 using the following relation/equation [26].

$$\text{Conductivity}\,\sigma_{dc} = \frac{t}{RA}\,\mathrm{S/cm}, \tag{9}$$

where t is the thickness, R is the resistance and A is the area of the film.

The variation of ln (σ) with respect to the applied voltage (V) at different temperature is shown in Fig. 9. Notably, the conductivity of the CeO_2 films was significantly influenced by both voltage and temperature. The mean conductivity (σ) of the CeO_2 films improved from 1.12×10^{-9} to 10.6×10^{-9} S/cm as the substrate temperature increased from 350 to 500 °C (Table 4). This conductivity range of CeO_2 films provided some insights on the semiconducting behaviour. The maximum conductivity of 10.6×10^{-9} S/cm was recorded for the film prepared at T_{sub} = 450 °C. The minimum bandgap and maximum crystallite size of CeO_2 film prepared at T_{sub} = 450 °C further assisted in the improved electrical conductivity of the film. The increase in conductivity is mostly due to the oxygen ion vacancies that are formed on the CeO_2 films during the spray deposition which is due to the partial dissociation of constituent elements. Furthermore, the reduction of grain-boundary scattering due to the higher grain size are responsible for the changes in the conductivity of CeO_2 film with temperature. The low conductivity of films at T_s = 500 °C is due to the insufficient grain growth of the films and oxygen deficiency. Activation energy (E_a) can be calculated using the following relation.

$$\sigma_{dc} = \sigma_0 \exp\left(\frac{-\mathrm{E_a}}{\mathrm{k_B T}}\right). \tag{10}$$

Figure 10 shows the variations of electrical parameters with substrate temperature. The activation energy could be influenced by the crystallinity and stoichiometry of the CeO_2 films. Moreover, the electronic conduction of ceria films are mostly due to the small polaron hopping mechanism [34]. At T_{sub} = 350 °C, the activation energy (E_a) was found to be 0.532 eV for CeO_2 film which decreased

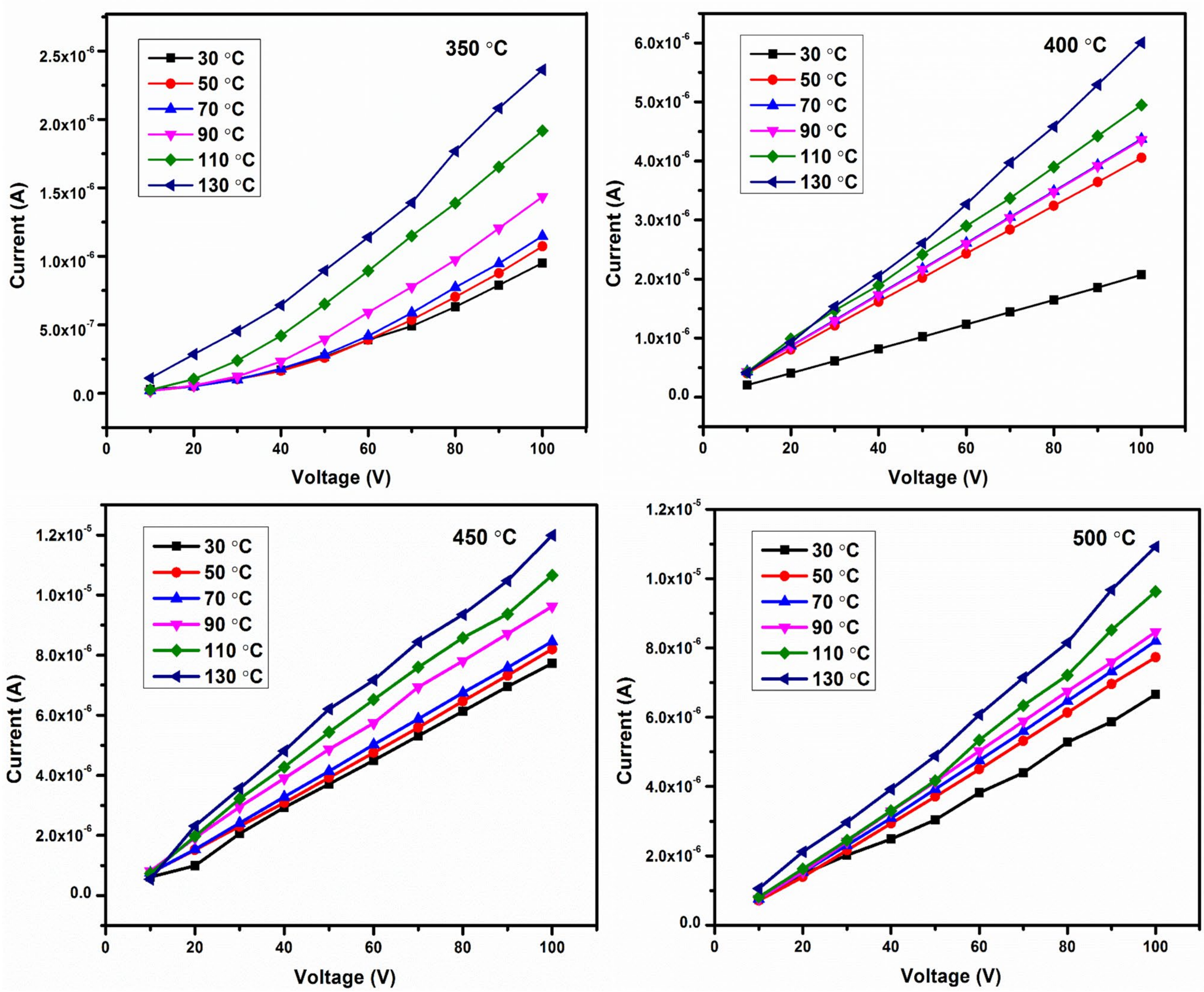


Fig. 8 I–V characteristics of CeO_2 thin films prepared at various temperature

Table 3 Electrical parameters of pure CeO_2 thin films for various substrate temperature

Substrate temperature (°C)	Resistivity, ρ (Ω cm)	Conductivity, σ (S/cm)	Activation energy, E_a (eV)
350	1.46×10^9	1.12×10^{-9}	0.532
400	2.26×10^8	4.87×10^{-9}	0.382
450	9.79×10^7	1.06×10^{-8}	0.306
500	1.06×10^8	9.61×10^{-9}	0.247

to 0.382, 0.306 and 0.247 eV for the T_{sub} of 400, 450 and 500 °C respectively. A similar range of electrical conductivity values (7.06–7.79 × 10^{-7} S/cm) and activation energy (0.377–0.648 eV) were reported for the ceria films prepared via JNSP technique by Suresh et al. [24]. The decline in activation energy with higher T_{sub} is attributed to the thermally activated electron transition from valance band to conduction band without any defects and traps. Ambilyn et al. observed similar results of decrease in activation energy with increasing substrate temperature [35]. The electrical parameters of the spray-coated CeO_2 films is strongly altered with substrate temperature.

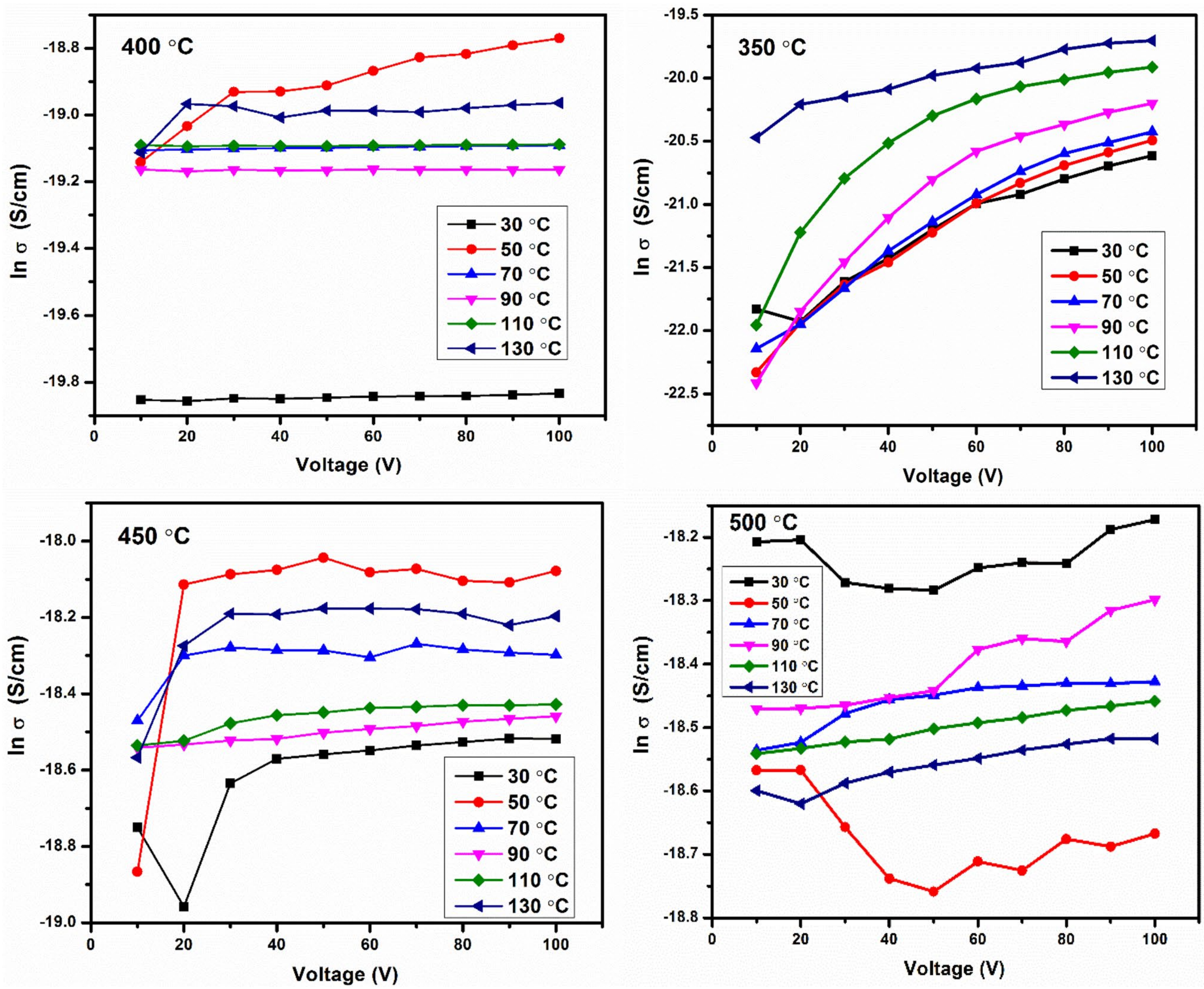


Fig. 9 Plots of voltage vs. ln (σ) of CeO_2 thin films coated at various temperature

Table 4 Calculated p-Si/n-CeO_2 junction diode parameters for various substrate temperature

Substrate temperature (°C)	Ideality factor (n)		Barrier height, Φ_B (eV)		Revers saturation current, I_o (A)		Photo-sensitivity, P_S (%)
	Dark	Light	Dark	Light	Dark	Light	
350	10.84	9.76	0.747	0.746	1.30×10^{-05}	1.34×10^{-05}	122.43
400	7.18	6.56	0.720	0.870	3.61×10^{-05}	1.17×10^{-07}	21.94
450	5.47	3.56	0.692	0.683	1.09×10^{-04}	1.50×10^{-04}	671.65
500	6.92	3.70	0.696	0.628	9.15×10^{-05}	1.25×10^{-03}	1093.75

3.6 I-V Characterization of p-Si/n-CeO_2 Diode

The schematic representation of the formed p–n junction is shown in Fig. 11. The photocurrent measurement can provide significant information about the photo-diode properties of the fabricated CeO_2 diode. The forward and reverse current of the p-Si/n-CeO_2 diodes were measured under light and dark conditions with the portable solar simulator having light intensity of 100 mW/cm^2. The distance between the device and illumination head was fixed at 10 cm. Figure 12 illustrates the I–V characteristics of the p-Si/n-CeO_2 diode for various substrate temperatures. Higher current values are expected for higher voltages when the diode is measured under light exposed condition. These results culminate the

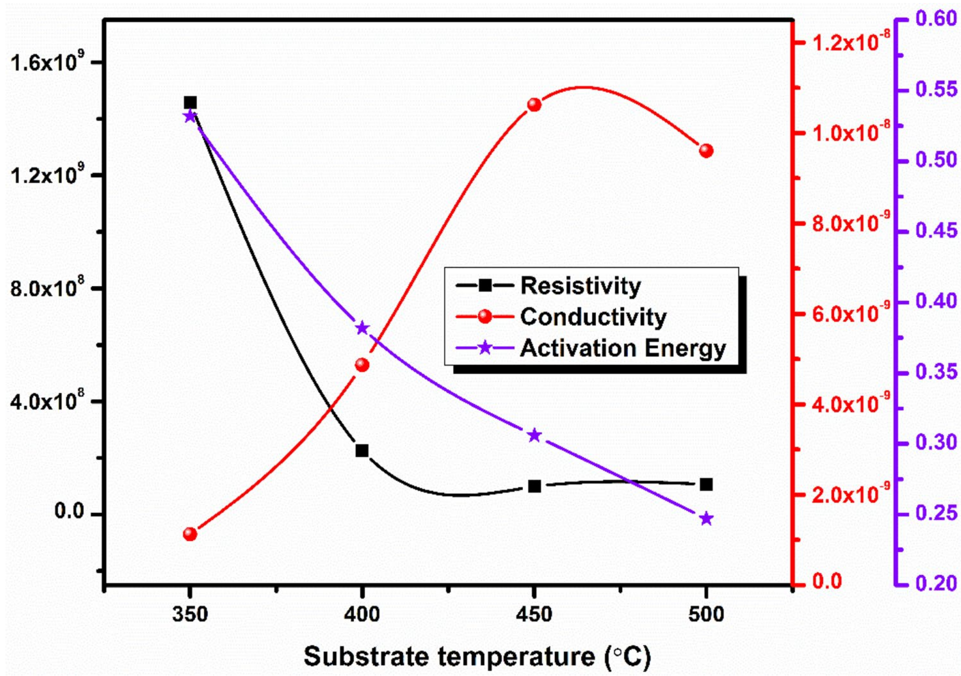


Fig. 10 Variations of electrical parameters of CeO_2 films with T_{sub}

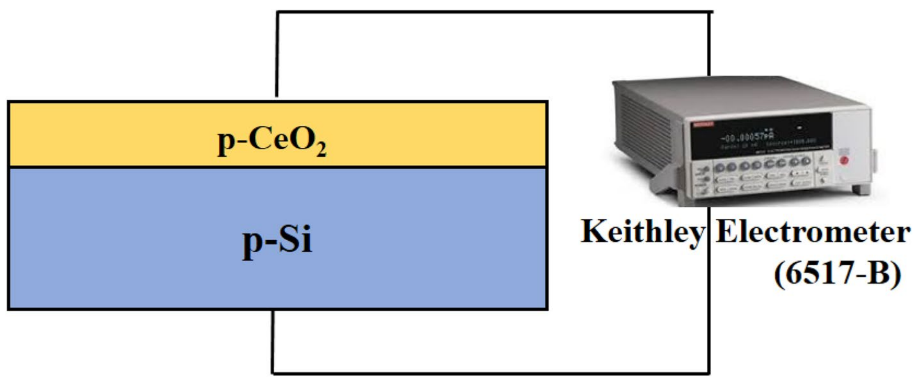


Fig. 11 Schematic representation of formed junction for p-Si/n-CeO_2 diode

photo-conducting behaviour of the CeO_2 diodes. Notably, the maximum photocurrent of 1.52×10^{-3} A was recorded at 3 V for T_{sub} of 500 °C. All the p-Si/n-CeO_2 diode revealed a similar behaviour of smaller reverse current and higher forward bias current, which demonstrated a good rectification behavior of the CeO_2 diodes. Conduction mechanisms of the CeO_2 fused device and its performance was studied by thermionic emission with the following equation [36–38].

$$I = AA * T^2 \exp\left(-\frac{q\varphi_B}{k_B T}\right)\left[\exp\left(\frac{qV}{nk_B T} - 1\right)\right], \tag{11}$$

where I_o is the reverse saturation current, q is the charge of an electron, V is the bias voltage, n is the ideality factor, Φ_B is the effective barrier height, A is the active area of the diode, k_B is the Boltzmann constant, T is the temperature and A* is the effective Richardson constant. The reverse saturation current (I_o) of the diode is generated by the drift of thermally generated charge carriers in the depletion region and it can be calculated using the following equation [39].

$$I_0 = AA * T^2 \exp\left(-\frac{q\varphi_B}{k_B T}\right). \tag{12}$$

The reverse saturation current of the CeO_2 diode was found to have improved from 1.17×10^{-07} to 1.25×10^{-03} A with higher substrate temperature. In fact the electron and holes dynamically created in the depletion region are accelerated towards the n-CeO_2 and p-Si region due to the applied voltage and this leads to a small reverse saturation current (Fig. 12). Figure 13 shows the semi-logarithmic plot for p-Si/n-CeO_2 junction diode for different temperature. The ideality factor (n) of the diode can be calculated

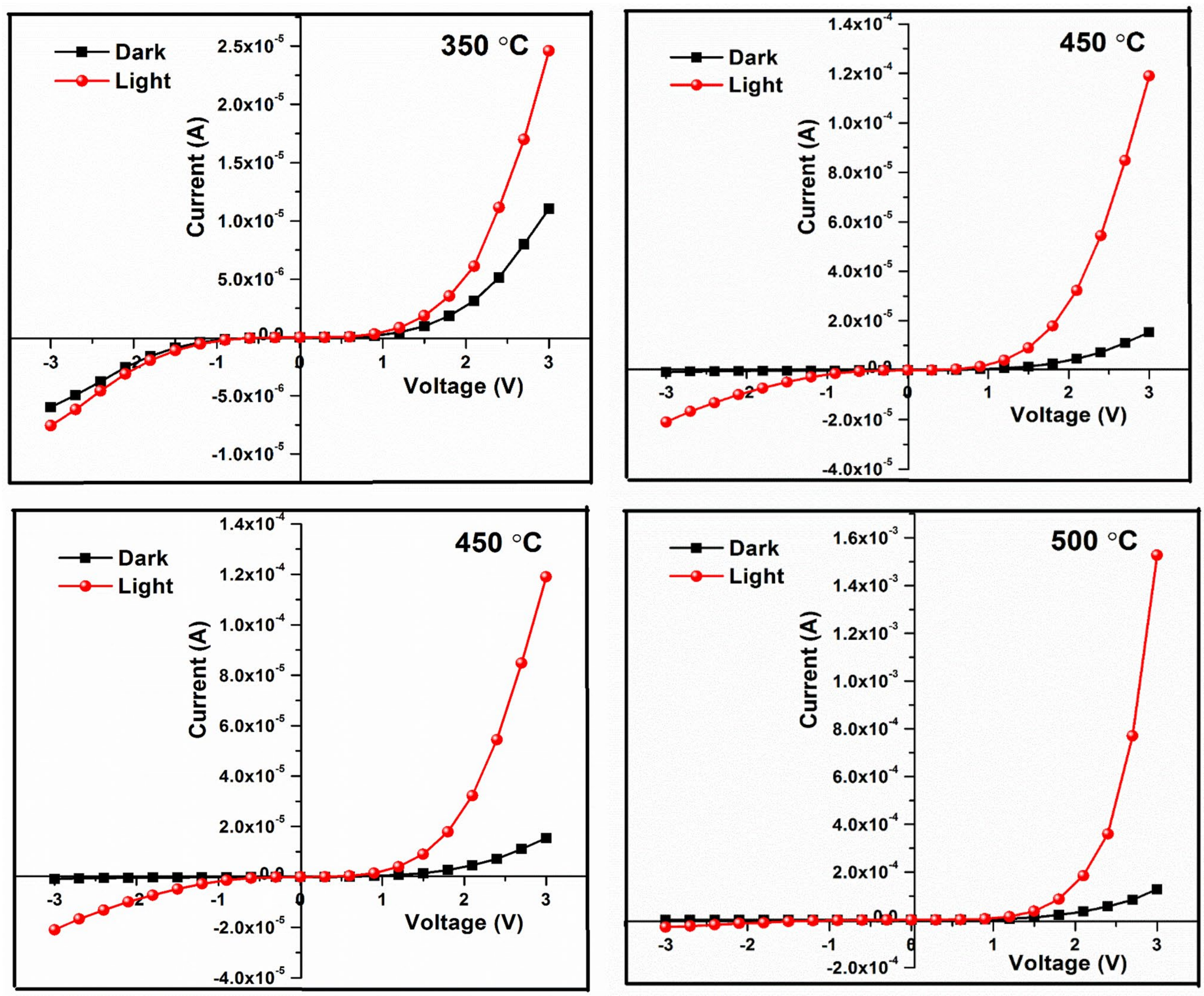


Fig. 12 I–V characteristics of p-Si/n-CeO_2 junction diode for different temperature

from the intercepts of semi-logarithmic plots using the following equation.

$$n = \frac{q}{k_B T}\left(\frac{d(V)}{d(\ln(I))}\right). \tag{13}$$

It is obvious from Table 4 that the ideality factor (n) of the CeO_2 diode was found significantly transformed with illumination condition and substrate temperature. The n values of CeO_2 diode reduced steadily for both the dark and light conditions up to higher T_{sub} = 450 °C and then increased slightly at 500 °C. The p-Si/n-CeO_2 diode fabricated with T_{sub} of 450 °C recorded a lower ideality factor of n = 3.56 under light condition. This result might be attributed to the formation of additional photo-generated carriers which is influenced by the external light absorbed in n-CeO_2 layer. Moreover, the charge separation and improved lifetime of photo-carrier have supported the cause [40]. The minimum bandgap of CeO_2 films at 450 °C have facilitated for the improved flow of charge carries from one side to another. Diode fabricated at lower T_{sub} (< 400 °C), recorded the highest ideality factor even in light condition due to the formation of weak photo-generated charge carriers. Moreover, owing to the presence of a thin native oxide layer (SiO_2) the barrier-inhomogeneity's, tunneling and image-force lowering [41–46]. The barrier height of the diode was calculated with the following expression.

$$\Phi_B = \frac{k_B T}{q} \ln\left(\frac{AA * T^2}{I_0}\right), \tag{14}$$

where $A^*$is the effective Richardson constant (32 A/cm^2 for p-Si).

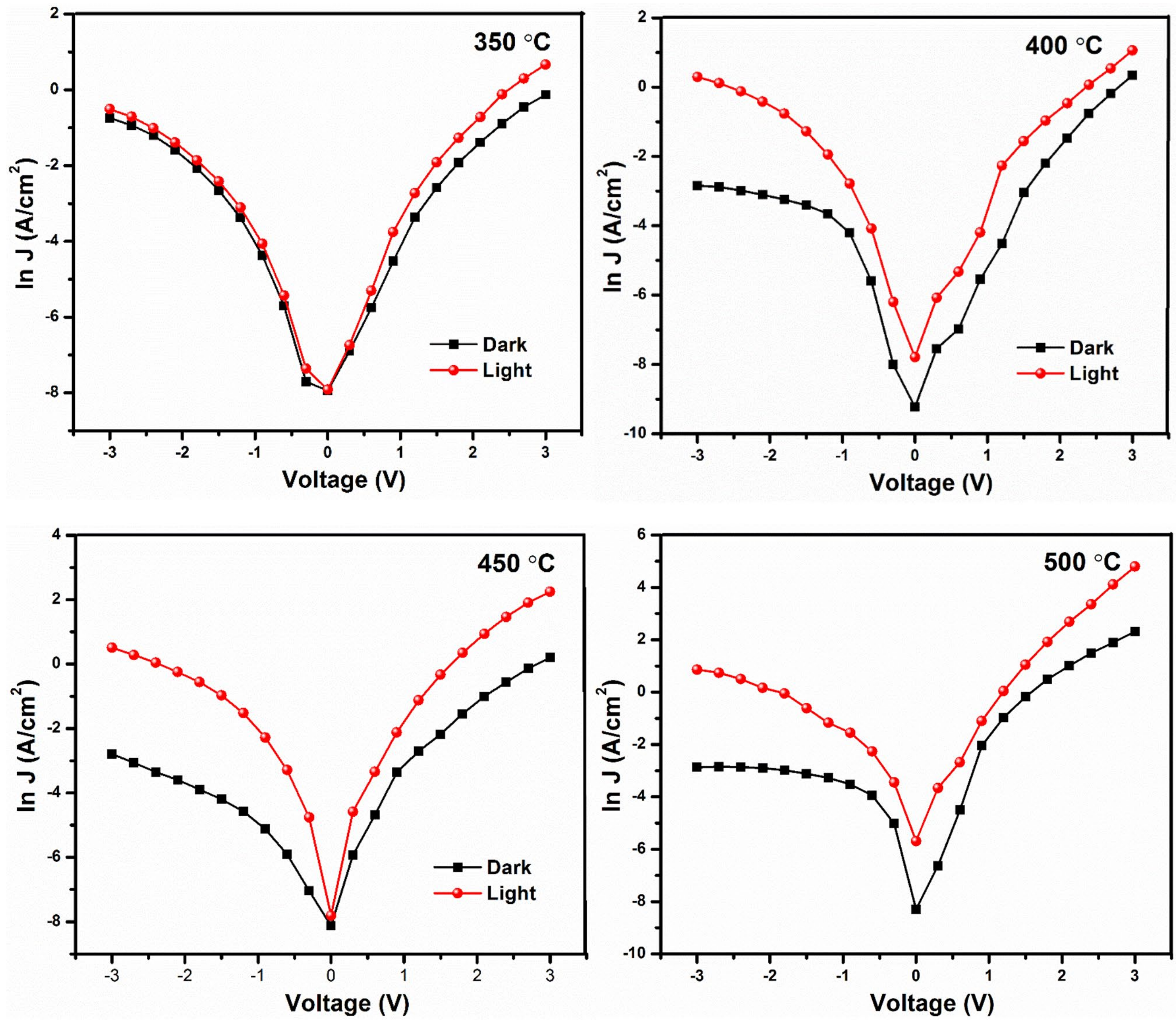


Fig. 13 Semi-logarithmic plot for p-Si/n-CeO_2 junction diode for different temperature

It is evident from Table 4, that the diode measured under 100 mW/cm^2 intensity exhibited smaller Φ_B values than those measured in dark conditions. The obtained barrier height varied between 0.747 and 0.628 eV with T_{sub} of the device. The barrier height of the two layer junction diode is mainly affected by the formation of the width of the depletion region. Furthermore, the distance between the diffused charge carriers (electrons and holes) reduces, resulting in a decreased electric field at the depletion region leading to a smaller potential barrier. The fabricated CeO_2 diode showed superior performance at higher temperature as the charge carriers had sufficient energy to easily overcome the higher patches [36–38, 41]. The photosensitivity of the diode can be calculated using the following relation [42].

$$P_s\,(\%) = \frac{I_{Ph} - I_D}{I_D} \times 100, \tag{15}$$

where I_{Ph} is the photocurrent and I_D is the dark current under dark and light conditions respectively. The photosensitivity of the diode increased with higher applied voltage. The maximum sensitivity of 122.43, 21.94, 671.65 and 1093.75% was obtained (at 3 V) for the corresponding T_{sub} = 350, 400, 450, and 500 °C. There are several factors including higher surface-to-volume ratio, surface defects, and more light absorption with less optical loss that could have contributed for the higher photosensitivity nature of p-Si/n-CeO_2 devices. Moreover, the prolonged photo generated charge due to the charge separation process at the surface states might be the possible reason for the improved

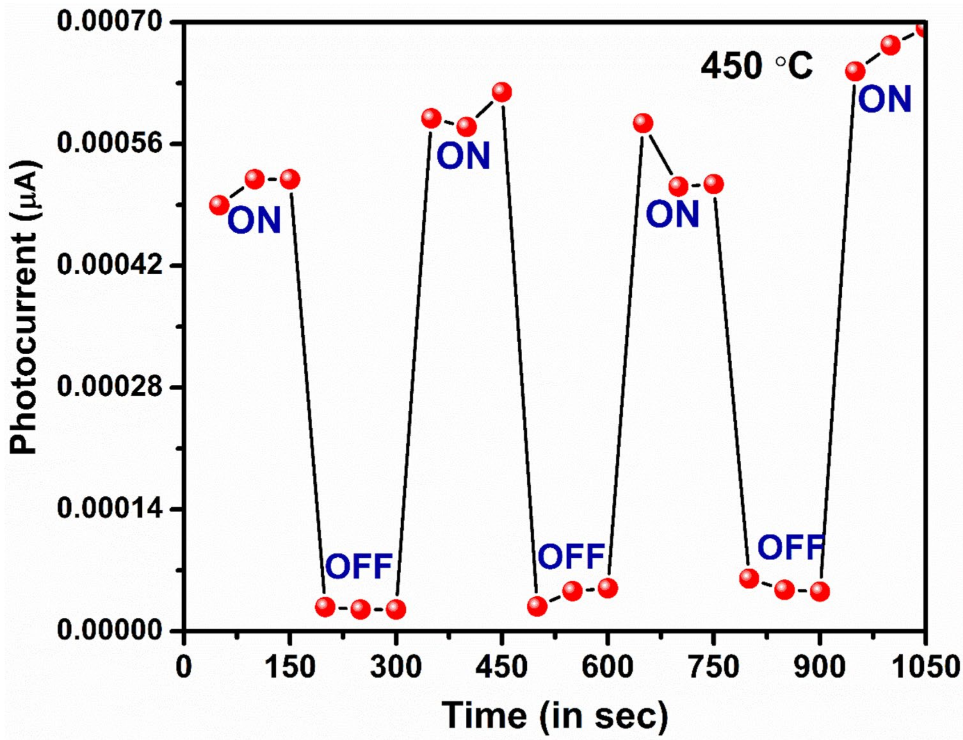


Fig. 14 ON–OFF switching response of p-Si/n-CeO_2 junction diode fabricated with 450 °C

photosensitivity [43]. The CeO diode with T_{sub} = 500 °C recorded a higher photosensitivity of 1093.75%. Such an outstanding performance under light exposed condition is attributed to the rapid separation of photo-generated electron–hole pairs influenced by the built-in electric field in the depletion region of p-Si/n-CeO_2 junction.

To further explore the photo-response of the device, we studied the time response (ON–OFF) for the p-Si/n-CeO_2 junction diode (with T_s = 450 °C) using portable solar simulator (PEC-L01) and Keithley electrometer (Model No. 6517 B). Under ON (light: 100 mW/cm^2) and OFF (dark: 0 mW/cm^2) conditions, the current values through the p-Si/n-CeO_2 diode was measured for the first 150 s under light exposed condition and likewise for the next 150 s in the darkness for a total time duration/dilation of 1050 s. During the ON and OFF state condition with 150 s each, the corresponding current values were noted at a time interval 50 s (at 3 V) for both the state separately as shown in Fig. 14. The diode under light exposed condition exhibited higher current values than in the darkness which implies that the diode under light illumination can produce larger number of charge carriers, which enhanced the flow of current. The ON and OFF state response of the p-Si/n-CeO_2 diode prepared at 450 °C have high stability, quick response time and good reproducing capability. From the overall diode performance, we conclude that the low-cost JNSP technique is suitable to produce high quality sensitive electronic devices.

4 Conclusion

A smooth CeO_2 thin film has been prepared on glass substrates by JNSP technique. The significance of substrate temperatures on the properties of nanocrystalline CeO_2 thin film have been investigated. A single phase cubic fluorite structure was observed for higher substrate temperatures (350–500 °C). The average crystallite size was found to vary in the range of 9.7 and 17.4 nm. FE-SEM micrographs revealed an inter-connected network-like crystal grains without any crack. CeO_2 film at 450 °C recorded a maximum optical absorption in both UV and visible region. The calculated bandgap energy of CeO_2 films improved from 3.30 to 4.08 eV with substrate temperature. A higher electrical conductivity (1.06×10^{-8} S/cm) and lower resistivity (9.79×10^7 Ω cm) was obtained for T_s 450 °C films due to the smaller scattering in the grain-boundary. The p-Si/n-CeO_2 diode characteristics showed maximum photocurrent and lower ideality factor values (n) under light exposed condition. CeO_2 diode prepared at higher substrate temperature exhibited superior photosensitivity of 1093.75% at 3 V. Our results indicated that the spray coated CeO_2 thin films are highly sensitive with both temperature and light. Hence the p-Si/n-CeO_2 diode is highly appropriate for next generation photonic related applications.

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