Wireless Personal Communications
https://doi.org/10.1007/s11277-019-06380-4

Implementation of Low Power Null Conventional Logic Function for Configuration Logic Block

P. Rajasekar[1] · **Subash Kumar C. S.**[2]

Abstract
Todays, transistor level design plays major impact in the power consumption of the VLSI based design. The various logic design models are used to reduce the power consumption that includes synchronous and asynchronous design model. The operation of synchronous circuit is limited by the in phase factor of the clock pulse signal which is used to control the synchronous circuit. In contrast, asynchronous circuits are used widely because it causes low noise, require less power. It affects the less electromagnetic interference that allows reuse of the components. These asynchronous circuits are being implemented by Null Conventional Logic (NCL) which is a delay insensitive logic model. The Configuration Logic Block is the power consuming model in Field Programmable Gate Array (FPGA). This block contains the lookup table (LUT) and 27 fundamental NCL logic gates. To reduce the power consumption of this module, we use the Differential Cascade Voltage Switch Logic (DVSL). The power reduction is achieved in LUT by means of DVSL and minimizes the number transistors. This NCL, DVSL, FPGA logic element is simulated using 90 nm TSMC CMOS processing technology.

Keywords Configuration logic block · Delay-insensitive circuits · Differential Cascade Voltage Switch Logic (DCVSL) · NULL Conventional Logic (NCL)

1 Introduction

According to the Semiconductor Industry Association (SIA) statements in 1997, synchronous circuit design model suffers the increase of clock frequency, clock distribution, clock rate, feature size, excessive power consumption and circuit complexity. To overcome the above limits, synchronous design model uses the sense amplifier logic. This logic is an improved design

✉ P. Rajasekar
rajasekarkpr@gmail.com

Subash Kumar C. S.
subashkumarcs@gmail.com

[1] Department of Electronics and Communication Engineering, Narayana Engineering College, Gudur, Andhra Pradesh 542 101, India

[2] Department of Electrical and Electronics Engineering, PSG Institute of Technology and Applied Research, Coimbatore, Tamil Nadu 641 062, India

Published online: 25 April 2019

model of Wave Dynamic Differential Logic (WDDL), Masked Logic using Fourier Transform (MLFT), two spacer alternating Dual rail circuit, Dual rail Random Switch Logic and Masked Dual rail pre-charge Logic. To implement the precious operation, precise timing control plays vital role. However, it suffers from glitches, early propagation and hazards of timing control issues, and also increasing demand of power efficient, noise resistant and high performance in digital design. It requires the new alternate design model where the designer should concentrate in effective design approach [1, 2].

It is found that an asynchronous circuit approach solves these major industry problems. The designer concentrates to develop new ideas and design approach. In general, the System on chip (SOC) technology may very well support the implementation of asynchronous model design. The Intellectual Property (IP) blocks may create using the SOC technology, which are the reusable building blocks of IC design. The IP blocks based system designs are plug and play assembly principles that leads to reduce the design time, testing etc. So, the system architecture point of view, the asynchronous design is much easier design model rather than synchronous design to build the SOC. It totally avoids the interfacing of multiple clock models [1, 2].

This asynchronous model is grouped in two category namely, bounded delay model and delay insensitive model. From these, delay insensitive approach gives enormous support to build the asynchronous design. The Null Conversion Logic (NCL) type, which is one type logic in delay insensitive logic. The NCL based asynchronous logic design cannot be neglected because of controlling the noise resistant, power efficient and improve the performance [3]. NCL is an asynchronous logic design that uses the interaction of alternating DATA and Null wave fronts, also known as delay insensitive paradigm. The operation of NCL is only based on the available of input data and operates correctly. The quad rail logic or dual rail logic is used to reach the delay insensitivity in NCL. The synchronization is achieved by delay insensitive in NCL paradigm design and by handshaking signal in self-timed paradigm [1].

Clock-related information leakage can be either eliminated or reduced by the proposed NCL logic. Both of the synchronous and asynchronous design methods, the Return-To-Zero (RTZ) and Dual Rail encoding with the pre-charge method protocols are frequently used. Data independence with the better power consumption can be achieved by the dual-rail encoding logic and pre-charge logic uses the monotonic transition method to enhance the security.

Our proposed Null Conventional Logic uses the Dual-Rail encoding and Null state. NCL design logic follows the monotonic transitions between DATA and NULL. DATA is called as Data representation and NULL is called as Control representation. These two are utilizing quad-rail and dual-rail signaling methods that achieve the reduction of design complexity. The absence of clock provides to reduce the power consumption, noise and electromagnetic interference.

This paper is organized as follows: Sect. 2 describes the related works. Section 3 describes the NCL. Design model overview Sect. 4 describes the simulation results and Sect. 5 Discussion and Conclusion.

2 Related Works

It turns out the, broad research area in asynchronous design and also several design methodologies haven been proposed in last two decades. Current Mode logic (CML) and Dual-Rail Pre-charge logic (DRP) are existing logic used in synchronous circuits. The dual output model is used in this logic model. The power consumption doesn't depend

on the operated data. Three-Phase Dual-Rail pre-charge Logic (TDPL) [4], Sense Amplifier Based Logic (SABL) [5], and Wave Dynamic Differential Logic (WDDL) [6] falls in this category. Most of the semi-custom design flow model uses the dual rail pre-charge logic, because the power consumption is insensitive to the unbalanced load condition. To implement the Dual Rail pre-charge logic, dual spacer signals are used. These signals are encoded as two complementary wires and consume constant power. The glitches not disturb this logic methods but it requires the two balanced wires that leads the requirement of full custom design. So, these design model increases the design complexity and maintenance cost. Glitches are totally avoided an implementation of Masked Dual-Rail pre charge logic (MDPL) method, but in random masking method at the gate level design, the consumed power is randomized.

Sense Amplifier Based Logic (SABL) [5] uses a fixed amount of charge for energy transitions which is constructed on Dynamic and Differential logic (DDL). Charge sharing effect occurs in this logic, in addition, to achieve the constant power consumption in Differential pull down network, a differential input connects in all internal nodes to an output node. Wave Dynamic Differential Logic [WDDL] [7] method requires only standard cells, so it reduces design time cost compared to full custom design where it fails to compensate the power imbalance. In addition, small voltage swing model at output and constant current at the internal nodes were used in the CML style logic. This CML logic style is encountered in low power implementation since the energy consumption is half the value compares to DRP logic. To safeguard from power analysis attack, MOS Current Mode Logic (MCML) can be used. However, larger static power consumption is the main drawback of this logic style. To overcome this drawback, dynamic logic styles have been proposed as the alternate model. Dynamic Current Mode Logic (DyCML) [8] has been one of the best dynamic logic style models.

In Current Mode Logic (CML) has been widely used in the high speed application that uses the differential pair of current logic. The transistors are ON whether fully or partially. In CML, the value of the outputs depends on the current passing through the pair of wires. Here logic is determined by the current difference between the pair wire. Due to the static power dissipation and design complexity MCML is not mostly prepared in design. To reduce the power and enhance the performance of digital design dynamic current mode model is used [4–7]. Ma et al. [8] describes the current mode method to reduce the power. To solve the unbalanced load capacitance problem the Three-Phase Dual-Rail pre charge logic (TDPL) [4] based on DRP style logic has been proposed. The TDPL adds an additional discharge operation and this additional function makes power consumption constant in every clock cycle. However, this logic style consumes two times more power than other DRP style logics [9]. So, we combined the DyCML and TDPL logic to achieve the better results in power as well as performance. The combined scheme logic is referred as Three Phase Dynamic Current Mode Logic (TPDyCML).

3 NCL Design Model

3.1 System Frame Work

The complete frame work of NCL system is shown in Fig. 1 which comprises the Delay Insensitive (DI) register, DI Combinational Logic, Completion detection and DI register. This is the general model structure for most of multi rail delay insensitive circuit design.

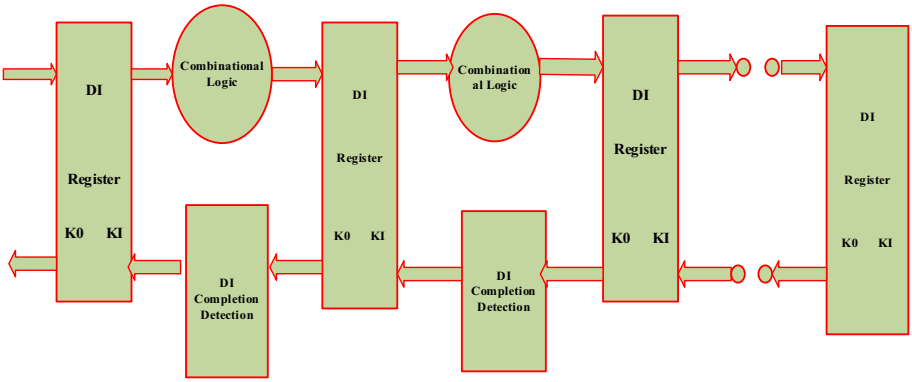


Fig. 1 NCL system overview

NCL logic gate is different comparatively traditional Boolean logic function. NCL achieves self-timed behavior on symbolic completeness of expression. The Boolean logic function output is valid only with in the reference time. But, NCL logic, dual rail and quad rail signals eliminates the time reference logic. Hence, time based digital design is completely discarded.

The logic parameters of dual rail and quad rail have been defined in terms of the mutually exclusive function. The Data D is referred by a two mutually exclusive wires, D^0, D^1. This Data may get any value from data set {data0, data1, NULL} that is used in dual rail signal. In similar manner, the Quad rail signal is defined as data set of {data0, data1, data2, data3, NULL}. Before going to implement the NCL, it should be verify that the following two criteria must be satisfied, namely, input completeness and observability.

In input completeness have two properties, NULL to DATA transition and DATA to NULL transition. The NULL to DATA transition occurs if and only if all inputs are switched over Null to Data. Similarly, output DATA to NULL occurs until all inputs have transitioned from DATA to NULL. Observable defines as every gate transition should be observed at one or more outputs.

Threshold gate (TH) with hysteresis is used in NCL logic elements. It consists of set and reset condition mode. The logic environment ensures that both conditions should not be occurring at the same time. In general, it is named as TH_{mn} gate, where m lies between the 1 to n, n as number of inputs. It defines that at least m of the inputs asserted before the output will be asserted. Before the output is de asserted all asserted input must be de asserted because of NCL logic gates are designed with hysteresis logic. So, as per the definition, set and reset condition can be used to represent the threshold gate equation $z = f + (g.Z^*)$ where f, g, Z* are set condition, complement of reset condition and past output value respectively. To satisfy the hysteresis condition, internal feedback path is used represent g.Z* [10, 11].

NCL date design has been implemented by using several CMOS scheme. These CMOS scheme are such as differential, dynamic, static, semi static. The real time computing application uses the dynamic implementation because it requires minimum data rate. So, the state information is kept an isolated node without use of feedback mechanism. Second, the differential design logic is used. It is almost similar to Boolean Differential Cascode Voltage Switch logic (DCVSL) gates [17]. Here both the output and its complement are available. The design can be used for minimizing area and faster execution. It uses the PMOS and NMOS transistor which results less transistor count. The use of PMOS gives less area and NMOS gives

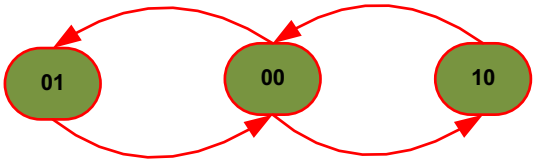


Fig. 2 Dual rail signalling protocol

faster operation [11]. The static gates tend to be faster with lower voltage operation capability whereas the semi-static gates are more area efficient [18]. In this paper we proposed a Differential Cascode Voltage Switch Logic based NCL gates for implement the LUT and compare the power to existing logics [2, 11].

3.2 Benefits of NCL Logic

There are so many benefits inherent by use of NCL model in asynchronous design. First and most benefit describe as the ease of design that means the circuit design behavior purely depends solely on the interconnection model. Since, the clock is eliminated in the design that completely removed clock skew and global coordination. In addition that power consumption, it doesn't have any spurious switching of transistors that leads to power reduction as well as NULL logic state is inherent state. Its action has taken into automatic power idle mode/state.

NCL uses the synchronized wave fronts of monotonic level transition and doesn't use edge triggering clock signal or clock pulses. It supports the simple technology migration which can easily changes from one technology model into upgraded technology model without additional overhead issues. Mostly physical environment variables such as temperature, voltage and manufacturing variations parameters affect the delay of design. But NCL takes as delay insensitive inherent that leads into automatic adaptation of variation in physical properties. In testing model, Stuck at 0 faults only can be examined and no need to verify the Stuck at-1 values. Because of the elimination of clock circuits design time, risks and circuit testing requirements are decreased [12].

3.3 Dual Rail Encoding

As mentioned earlier, NCL uses the dual rail which has two wires for single logic. In dual rail '0' and '1' are encoded as '01','10' values in two wires respectively. The code word logic 0 and 1 are transition via spacer that has the value of "00" in two wires. This dual rail signaling protocol is shown in Fig. 2.

The transition of logic signal code word '0' to '1' is passed via '00' spacer. The spacer state time is controlled by transient spacer control that takes the time insensitive. The control transient mode utilizes the very minimum time [13]. This is shown in Figs. 3 and 4.

In code word generation scheme, data path acknowledge takes longer time in spacer but in control path acknowledge scheme takes only short time. These spacer state timings are shown in Figs. 3 and 4.

Dual rail design model is derived from single rail model by using RTL based design. NCL design logic is implemented in two different implementation, namely NCL-D and NCL-X. The former integrates completion detection into the dual rail while later relies separate detection completion circuit. NCL-D has more conservative with respect to delay sensitive and NCL-X occupies more area with speed efficient. This dual rail logic allows achieving race free operation. It also has added feature of balanced power consumption, leads to resist the power

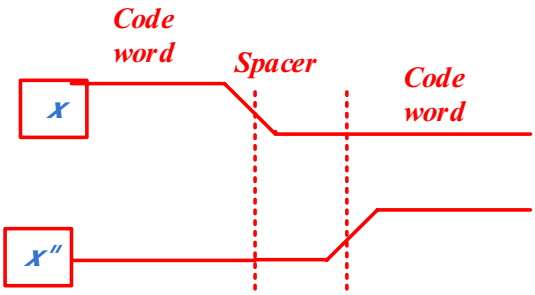


Fig. 3 Data path acknowledge spacer

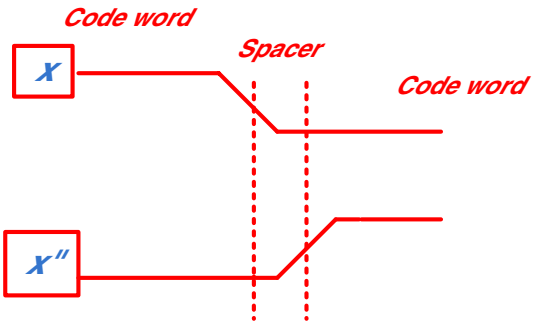


Fig. 4 Control path acknowledge spacer

Table 1 Dual rail encoding scheme

DATA	D^0	D^1
Data0	1	0
Data1	0	1
Null	0	0
Invalid	1	1

analysis attack. The alternating spacer protocol is introduced in dual rail to improve the security threats [14]. Though it has so many advantages, it occupies more area and increased power consumption compared to single rail logic.

Dual rail encoding logic wires are represented as D^0, D^1 and different states are as Data0, Data1, Null and Invalid. It is tabled in the Table 1.

The NCL dual rail logic function is expressed in terms Sum Of Product (SOP), for an example the AND gate function is defined as F = AB in Boolean logic where as in NCL Dual Rail F = A'B + AB' + A'B'. It uses the three SOP terms in NCL based rail 1, rail 0 AND function [11].

In general, there are 27 different logic function models derived for NCL static circuits. These 27 NCL Threshold circuit gates are denotes as the TH_{mnw}, where 'm' threshold value, 'n' no. of inputs and 'w' the weigh value. For an example TH12 gate has threshold value of '1' and number of input variable 2. In the listed of 27 NCL gates, three NCL gates namely, TH24comp, THand0, THxor0 are not TH gates. All NCL gates are listed in Table 2. From these, some gates are resettable gate because these gate's output can be asserted/deserted when the reset input is asserted [6].

Table 2 Fundamental NCL gates

S. no.	NCL gate	Function
1.	TH12	A + B
2.	TH13	A + B + C
3.	TH14	A + B + C + D
4.	TH22	AB
5.	TH23	AB + AC + BC
6.	TH24	AB + AC + AD + BC + BD + CD
7.	TH33	ABC
8.	TH34	ABC + ABD + ACD + BCD
9.	TH44	ABCD
10.	TH23w2	A + BC
11.	TH24w2	A + BC + BD + CD
12.	TH24w22	A + B + CD
13.	TH33w2	AB + AC
14.	TH34w2	AB + AC + AD + BCD
15.	TH34w22	AB + AC + AD + BC + BD
16.	TH34w3	A + BCD
17.	TH34w32	A + BC + BD
18.	TH44w2	ABC + ABD + ACD
19.	TH44w22	AB + ACD + BCD
20.	TH44w3	AB + AC + AD
21.	TH44w322	AB + AC + AD + BC
22.	TH54w22	ABC + ABD
23.	TH54w322	AB + AC + BCD
24.	THxor0	AB + CD
25.	THand0	AB + BC + AD
26.	TH24comp	AC + BC + AD + BD
27.	TH54w32	AB + ACD

3.4 Proposed NCL Logic

The implementation of the logic in VLSI design is majorly cauterized as the static, semi static, DCVLS and DNCL. Static design is already defined and validated in transistor logic design.

Static logic consists of SET, RESET, HOLD0, HOLD1 network; whereas semi-static logic consists of SET, RESET and feedback inverter. The semi static circuit is shown in Fig. 5. In this logic, the reset function is implemented in pull-down network, and Set function is implemented in pull up network. Neither set nor reset function true the feedback inverter keeps the charge as it is [15]. Function and complement functions are implemented using differential logics that use two output rails. PUN is complement of the PDN model that gives less area design in PUN in PMOS transistor. The function implementation is realized by NMOS, which results in faster and smaller design and shown in Fig. 6. In another design is shown in Fig. 7, Differential NCL gate structure which is designed by separate Set and Reset condition [16].

The Different logic types features are listed in Table 3 in design of CMOS structure in pull up and pulls down network model. In Figs. 8, 9 and 10 which are shown as the

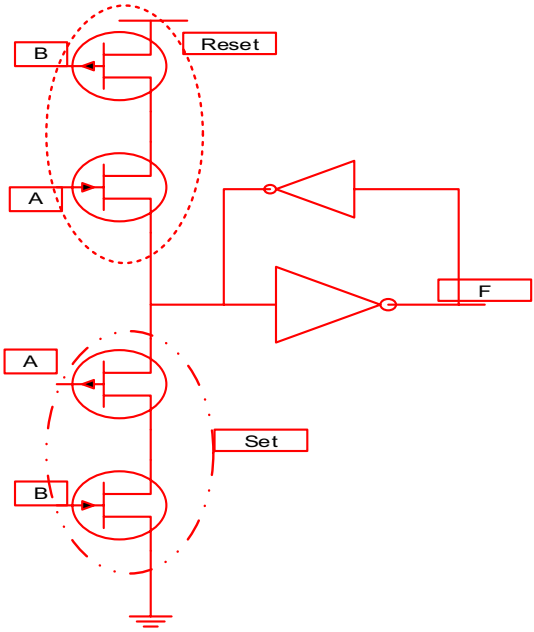


Fig. 5 Semi static CMOS TH_{22} gate

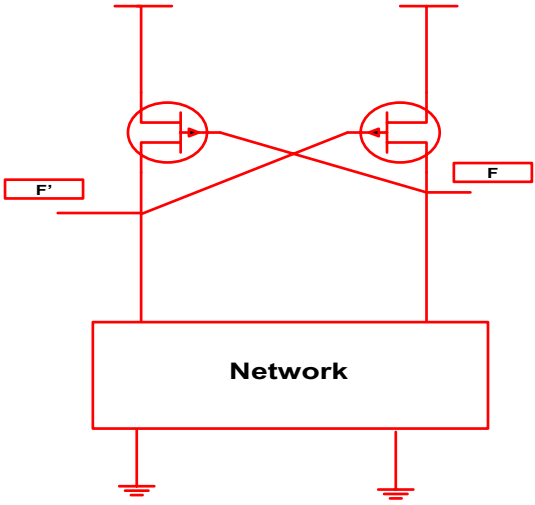


Fig. 6 DCVSL gate architecture

implementation of TH23 NCL gate in different logic methods and calculate the power consumption of the basic gate which is to be use in the Configuration block design.

A DCVSL requires that each input is provided in complementary format and produces complementary output in turn. In these logic PMOS area is minimized and all functions are realized in NMOS, which results in both a faster and smaller design [15].

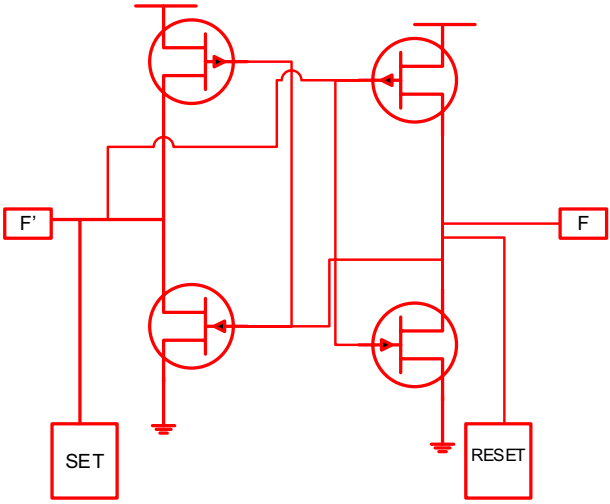


Fig. 7 Differential NCL gate architecture

Table 3 Different logic types features

Logic type	Module
Static NCL	Set, reset, Hold0, Hold1
Semi static NCL	Set, reset, feedback inverter
DCVSL	Complementary pull up pull down, combined set and reset
DNCL NCL	Complementary pull up pull down, separate set and reset condition.

4 Simulation Results and Discussion

The design has been simulated and analyzed using Tanner EDA's design tool with 90 nm technology. The proposed NCL logic style is analyzed in basic TH_{23} NCL gate and derived 2–1 multiplexer. Further the proposed NCL logic style's power comparison has been analyzed in AND TH_{23} gate. The sample design has been implemented using different NCL logic style, and optimization, effectiveness analyzed in terms of number of transistor used. It is also validated by power consumption. Table 4 shows that the number of transistor is used to build up the basic gate. From the Table 4, Figs. 11 and 12 proposed DCVSL reduced 38% of transistor compared to static design. Similarly, proposed DCVSL reduced the 8.33% transistor compared to semi static. Since, the proposed design structure changes in pull up and pull down network, the number of transistor usage is minimized.

Based on the above analysis, various basic gates are implemented with different logic style. The power consumption is measured and tabulated in Table 5. It is observed that the proposed NCL consumes less power. The maximum power consumption reduction in AND gate is of 84.32%, and minimum power reduction is 58.79%. Similarly power reduction in OR gate is 79.75% to 47.56% and mux takes reduction of approximately 4%. These gates are mainly used the building block of configuration logic block. So, the power consumption, area have been reduced minimum 4% to maximum of 84.32%. These are illustrated in Figs. 13 and 14. The same is also tabulated in Tables 5 and 6.

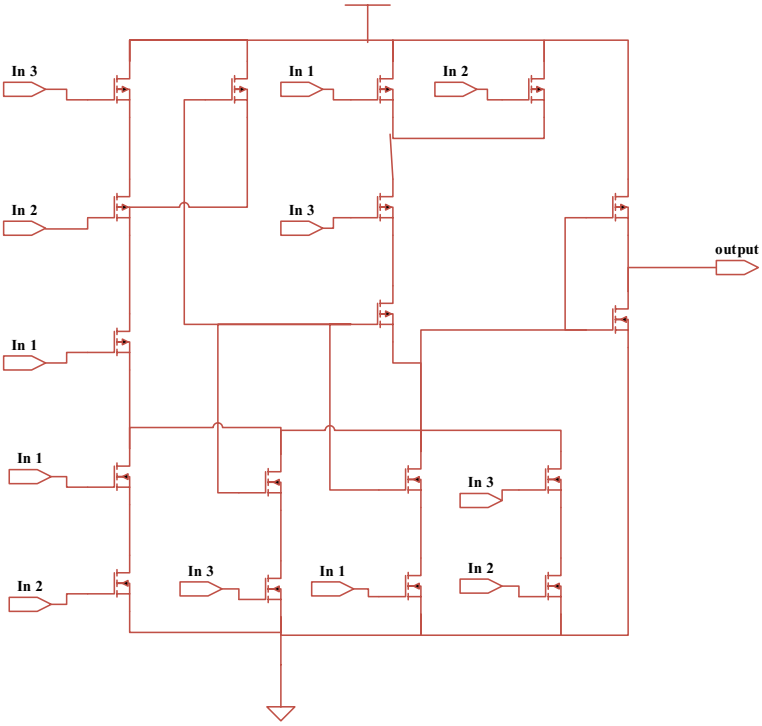


Fig. 8 Static TH23 NCL gate

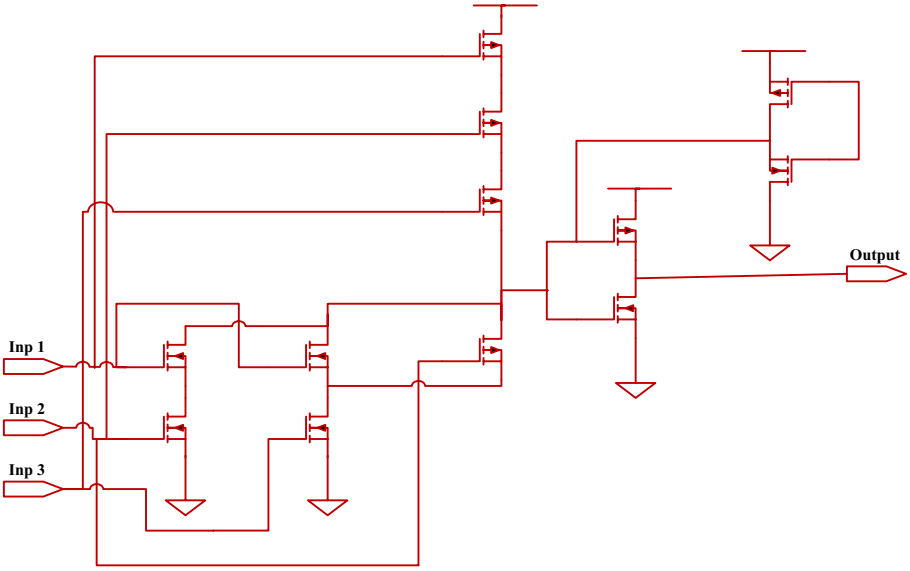


Fig. 9 Semi-static TH23 NCL gate

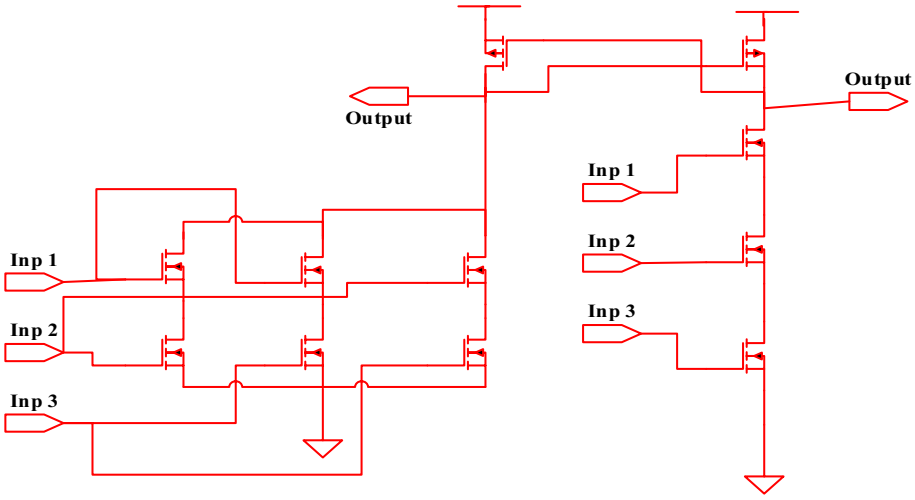


Fig. 10 Proposed DCVSL based TH23 NCL gate

Table 4 Transistor usage

Logic type	No of transistor
Static TH_{23}	18
Semi-static TH_{23}	12
Proposed DCVSL TH_{23}	11

Fig. 11 Transistor usage reduction in %

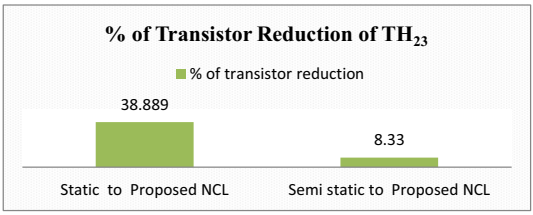
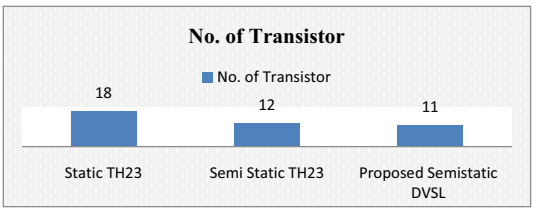


Fig. 12 Number of transistor used



It is observed from the table and Fig. 14, power reduction achieved as 84.32% against WDDL logic in AND gate, 79.75% in OR gate, 67.28% in NAND gate. The proposed logic design is achieved as 70.58%, 60.57%, 68.65% and 2.8% of AND, OR, NAND, and

Table 5 Power reduction in various logic function with different logic style

Logic	Power in μW				
	AND gate	OR gate	NAND gate	NOR gate	2:1 MUX
WDDL	13.95	14.47	4.83	4.70	
SDMLp	7.41	7.43	5.04	4.50	
SCMOS	5.29	5.62	3.63	3.32	
NCL	2.18	2.93	1.58	4.63	4.58

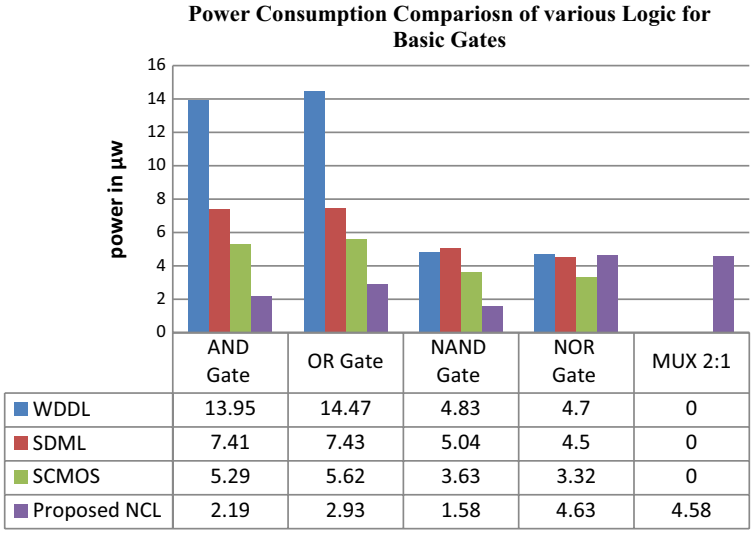


Fig. 13 Power consumption of various logic function

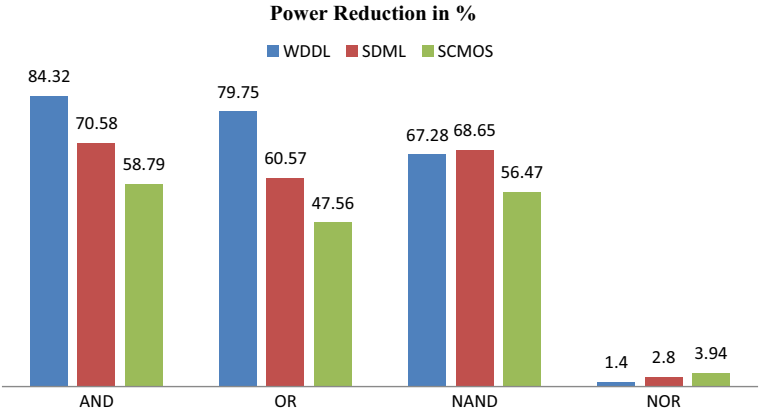


Fig. 14 NCL power reduction comparison with various logic function in different logic styles

Table 6 Power reduction % comparison of NCL with various logic

Logic	AND gate	Power in µW								
		% Power[a]	OR gate	% Power[a]	NAND gate	% Power[a]	nor gate	% Power[a]	2:1 MUX	% Power[a]
WDDL	13.95	84.32	14.47	79.75	4.83	67.28	4.20	1.4	–	
SDMLp	7.41	70.58	7.43	60.57	5.04	68.65	4.50	−2.8	–	
SCMOS	5.29	58.79	5.62	47.56	3.63	56.47	4.82	3.94	–	
NCL	2.18	–	2.93		1.58	–	4.63	–	4.28	4.88
DDCVS	–		–		–		–		4.70	4.25
MCML	–		–		–		–		4.50	

[a]% of power reduction of proposed NCL with corresponding logic

NOR gates respectively in SDML design. SCMOS logic design consumes more power of 58.79%, 47.56%, 56.47% of AND, OR, and NAND gates against the proposed NCL design. Hence, we concluded that the NCL logic style is comparatively better option to others.

5 Conclusion

The proposed DCLVL based NCL based logic gates can be implemented by less number of transistors compared to all other transistor model. In basic logic design consumes 15.68% power in AND gate as the best case and 41.81% power consumed in worst case. It takes the advantages of area occupation in semiconductor design. It achieves the power reduction almost 50% compared to the conventional design style. These basic logic gates model and multiplexer design modules are the fundamental building blocks of LUT and CLB in FPGA design. From the above simulation results the proposed NCL is best suited for LUT and CLB models.

References

1. Al-Assadi, W., & Kakarla, S. (2009). Design for test of asynchronous NULL convention logic (NCL) circuits. *Journal of Electronic Testing, 25*(1), 117–126.
2. Allam, M., & Elmasry, M. (2001). Dynamic current mode logic (DyCML): A new low-power high-performance logic style. *IEEE Journal of Solid-State Circuits, 36*(3), 550–558.
3. Bucci, M., Giancane, L., Luzzi, R., & Trifiletti, A. (2006). Three-phase dual-rail pre-charge logic. In *Cryptographic hardware and embedded system CHES 2006* (Vol. 4249, pp. 232–241). Yokohama, Japan: International Association for Cryptologic Research.
4. Datta, D., Mitra, P., & Sen, A. (2013). Low power configuration logic block design using asynchronous static. *International Journal of Soft Computing and Engineering, 3*(1), 260–263.
5. Dugganapally, I., Al-Assadi, W., Tammina, T., & Smith, S. (2008). Design and implementation of FPGA configuration logic block using asynchronous static NCL. In *Region 5 IEEE conference* (pp. 1–6). IEEE.
6. Kim, H., Rozic, V., & Verbauwhede, I. (2012). Three phase dynamic current mode logic: a more secure DyCML to achieve a more balanced power consumption. In *13th international workshop, WISA* (pp. 68–81). Jeju Island, Korea: Springer Link.
7. Lee, H., & Kim, Y. (2013). Low power null convention logic circuit design based on DCVSL. In *IEEE 56th international midwest symposium on circuits and systems (MWSCAS)* (pp. 29–32). Ohio Union, USA: IEEE.
8. Ma, J., Kapoor, H.K., Krilavicius, T., Man, K.L., Zhang, N., Lim, E.G., Jeong, T.T., Guan S.U., & Seon, J.K. (2011). Specification and analysis of NCL circuits. *Engineering Letters, 19*(3).
9. Moreira, M., Arendt, M., Moraes, F., & Calazans, N. (2015). Static differential NCL gates: toward low power. *IEEE Transactions on Circuits and Systems II-Express Briefs, 62*(6), 563–567.
10. Parsan, F., & Smith, S. (2012). CMOS implementation comparison of NCL gates. In *IEEE 55th International midwest symposium incircuits and systems (MWSCAS)* (pp. 394–397). IEEE.
11. Parsan, F., & Smith, S. (2012). CMOS implementation of static threshold gates with hysteresis: A new approach. In *IEEE IFIP 20th international conference* (pp. 41–45). Santa Cruz, USA: IEEE.
12. Ramakrishnan, L., Chakkaravarthy, M., Manchanda, A., Borowczak, M., & Vemuri, R. (2012). SDMLp: On the use of complementary pass transistor logic for design of DPA resistant circuits. In *IEEE international symposium on hardware-oriented security and trust (HOST)*, San Francisco (pp. 31–36).
13. Smith, S. (2007). Design of an FPGA logic element for implementing asynchronous NULL convention logic circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 15*(6), 672–683.
14. Sokolov, D., Murphy, J., Bystrov, A., & Yakovlev, A. (2004). Improving the security of dual-rail circuits. In *CHES* (pp. 282–297).
15. Tanimura, K., & Dutt, N. (2012). *A standard cell-based DPA attack countermeasure using homogeneous dual-rail logic (HDRL)*. Irvine: University of California.

16. Tiri, K., & Verbauwhede, I. (2004). Charge recycling sense amplifier based logic: securing low power security ICs against DPA [differential power analysis]. In *Proceeding of the 30th european conference in solid-state circuits* (pp. 179–182). IEEE.
17. Wu, Jun, Shi, Yiyu, & Cho, M. (2012). Measurement and evaluation of power analysis attacks on asynchronous S-box. *IEEE Transactions on Instrumentation and Measurement, 61*(10), 2765–2775.
18. Yancey, S., & Smith, S. (2010). A differential design for C-elements and NCL gates. In *53rd IEEE international midwest symposium in circuits and systems (MWSCAS)* (pp. 632–65). IEEE.

P. Rajasekar received the B.E. degree in Electronics and Communication Engineering from the Sri Krishna College of Engineering and Technology, Bharathiar University, Coimbatore, Tamil Nadu, India, in 2003, M.E. degree in Applied Electronics from PSG College of Technology, Coimbatore, Anna University, in 2008 and Ph.D. degree in Information and Communication Engineering from the Anna University, Chennai, in 2018. His current research interests include cryptography, Low power Architectural design in FPGA, Network security, Encryption process. He is currently working as Professor, Narayana Engineering College, Gudur, Nellore, and Andrapradesh. He is a member of International Association of Engineers, The Society of Digital Information and Wireless Communications, IASTER.

C. S. Subash Kumar received his B.E. degree in Electrical and Electronics Engineering from Kumaraguru College of Technology in 2002. He received his M.E. degree in Electrical Machines from PSG College of Technology in 2008. He had completed his Ph.D. in the area of power quality in the field of Electrical Engineering. Currently, he is an Associate Professor in the Department of Electrical and Electronics Engineering at PSG Institute of Technology and Applied Research, Coimbatore, Tamil Nadu, India. His research interests include power electronics applications in power system and active power filters for power conditioning, Industrial Automation. He is the Life Member of ISTE and member of IEEE.