Performance Analysis of ST-Type Module for Nearest Level Control Scheme Based Asymmetric 17-Level Multilevel Inverter Fed Single-Phase Induction Motor

P. Ramesh, M. Hari, M. Mohamed Iqbal, K. Chitra and D. Kodandapani

Abstract A novel design of ST (Square type)-type module for asymmetric multilevel inverter (MLI) fed induction motor is approached in this research. The two back-to-back ST-type inverters and few different switching modules produce 17-level output by 12 switches with four unequal DC sources and filter. The advantages of this proposed technique are first, output voltage of the inverter can be is increased by cascading the inverter module. The main aspect of proposed inverter is natural conception of both +ve and −ve voltages without any auxiliary circuit. With the Nearest Level Control (NLC) switching strategy, good quality of output voltage with lower total harmonic contents can be accomplished. The response of the proposed module is analyzed by using MATLAB/SIMULINK. The simulation results are validated with prototype experimental results.

Keywords ST-Type back-to-back inverters · Asymmetric multilevel inverter · Nearest level control

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1 Introduction

Various industrial applications have started to require higher power rating machines [1] and many utility applications required medium voltage and high voltage levels. It is difficult to associate just single power semiconductor switch legitimately for the medium voltage drives. As a result, an alternative solution for large and medium voltage situations, a structure of multilevel inverters is preferred [2]. The multilevel inverters are highly suitable for the usage of renewable energy sources [3]. The vast majority of renewable power sources like photovoltaic, wind, and fuel cells are effectively interfaced with MLI topology for high-power applications [4, 5]. With the multiple dc sources and proper switching combinations of power switches, the high-power output voltage is achieved. Power semiconductor devices voltage ratings depend on only the total peak value of voltage source that is connected to the device. Multilevel inverters are categorized as diode clamped, flying capacitor, and *H*-bridge cascaded types. In [6], *T*-source with most extreme steady boosted PWM control was conferred. In [7], an Envelop Type (*E*-Type) asymmetric multilevel inverter is proposed and PWM (Pulse Width Modulation) scheme is used. These are used in high voltages and high-power applications and have reduced Total Harmonic Distortion (THD). In [8] a scheme for nearest level control (NLC), sub-module is proposed. The value of THD is reduced due to large number of steps present in the output voltage. In [9], the system used for 1-phase 5-level cascaded *H*–bridge multilevel inverter, constant *K*- filter used at a different cutoff frequency, output voltage, and current harmonic distortion is analyzed at different conduction angles. In [10], various topology comparisons of asymmetric CHB, SHE, NLC, PWM, multi-carrier method are presented and it produces excellent output voltage quality and lower THD using NLC scheme.

The branch current replication based energy balancing technique for the modular multilevel matrix converter (M3C) is proposed [11]. A new topology has presented a Simplified NLC based voltage balancing method [12].

Modular MLI converter is used under normal and emergency conditions. LSPWM balancing algorithm is used in this module [13]. NLC scheme is used for closed-loop and industrial applications. In [14], proposed section is a new module multilevel inverter using NLC technique by reduced power switches. In [15], a Level Doubling Network (LDN) topology produces a double number of output voltage levels and it produces self adjusting during positive and negative cycles with no closed loop control/algorithm. In [16], a submodule hybrid cascaded multilevel inverter (HCMLI) with gate drive requirement switches are reduced and efficiency will be increased. It is used for lower voltage applications. In [17], the harmonic reduction techniques for 2-level inverter fed induction motor were presented. The PWM technique is used for the performance of multilevel inverter are presented [18, 19].

The objective of this paper is to generate 17-level output voltage with 12 switches and also to get good quality of output voltage of the MLI with reduced number of switches. This paper also describes a novel design of square *T*-type multilevel

inverter fed induction motor using NLC scheme to achieve maximum voltage levels and improve economic implementation and high quality of power [20, 21].

2 Proposed System

2.1 Block Diagram of NLC Controller

Figure 1 shows that asymmetrical multilevel inverter can be modulated with nearest level control (NLC). In this method, the voltage levels are chosen nearest to the reference voltage [12]. The nearest level controller gives an excellent output voltage quality, and it produces an inverse relationship between frequency and distributed power from each unit.

NLC based inverter is used to produce higher number of levels and to simplify the calculation steps.

Figure 2 shows a point of reference voltage (V_{ref}) and then round off to the nearest voltage level (V_{aN}). The sampling is rehashed for each sample time (T_s) [20].

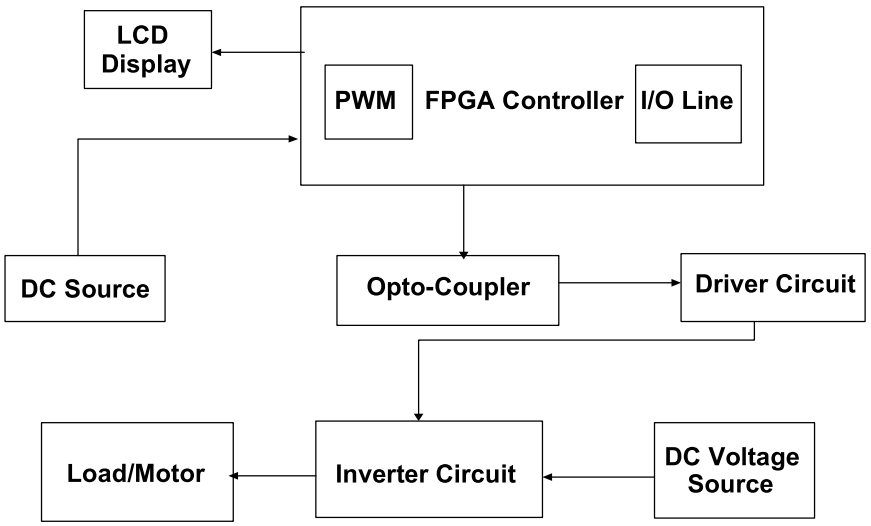

Fig. 1 Block diagram of NLC controller

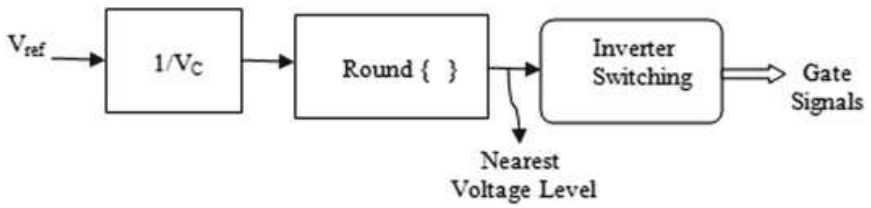

Fig. 2 Control diagram of NLC

The proposed module produces 17-levels such as eight positive, eight negative and one zero level without any need of additional circuit for creation of negative voltage levels. The NLC uses an excellent output voltage quality, and it produces an inverse relationship between frequency and distributed power from each unit.

2.2 Circuit Configuration

Figure 3 shows the proposed circuit diagram for 17-level ST–type inverter. The circuit configuration of proposed 17-level inverter consists of four unequal DC sources (two 10 V and two 30 V) and less number of power electronic switches (12 switches), which is parallel to filter and single-phase induction motor. Surrounding switches (S_1–S_6) are single-directional switches and middle switches (S_7–S_9)

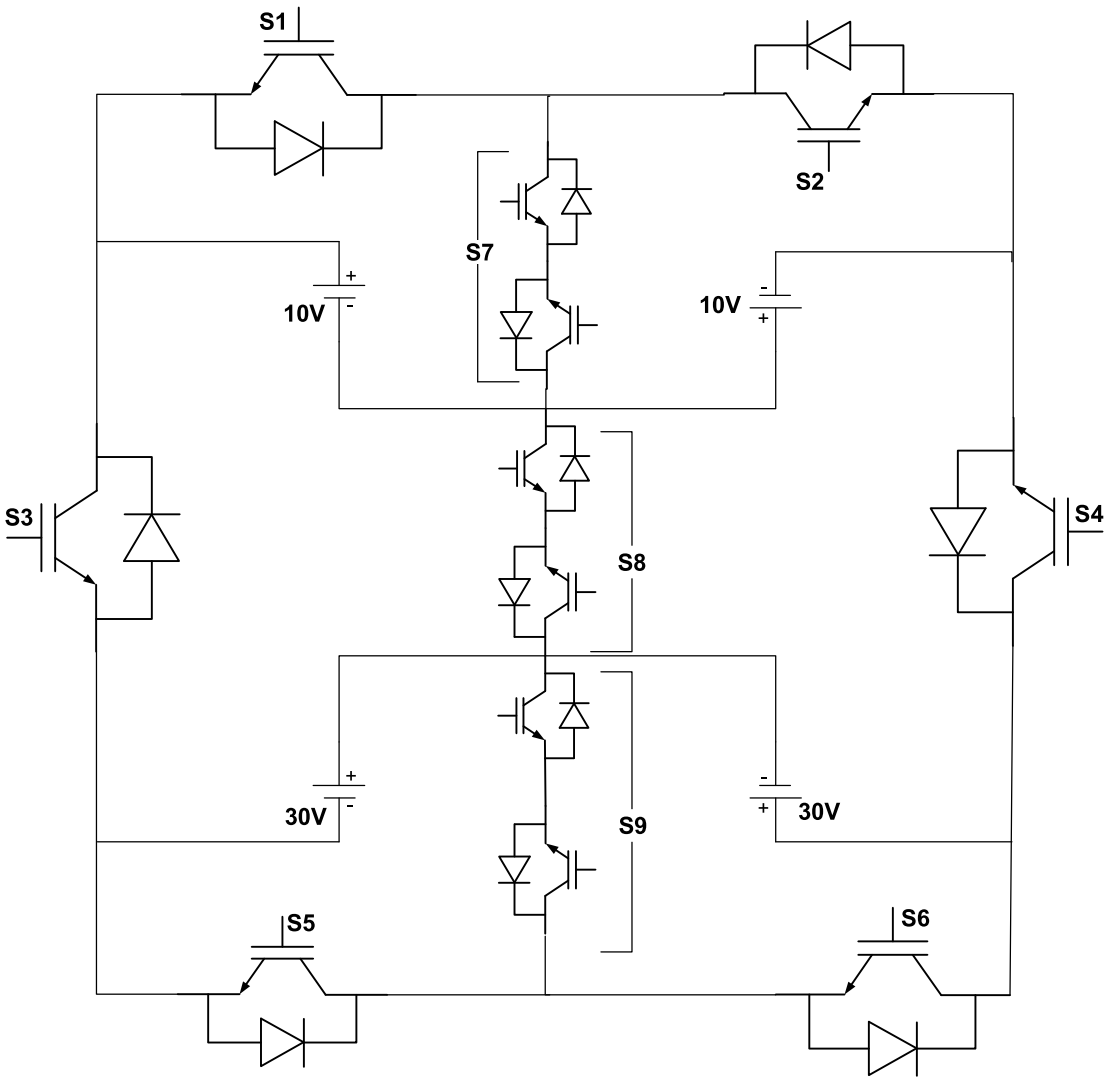

Fig. 3 Proposed 17-level inverter circuit [20]

are two-directional switches. The different modes of operations are used to define the current flow in switching components to obtain the various output voltage levels across "*A*" and "*B*". It consists of two levels of output voltages, positive and negative level, each level consist of eight modes of operation [20]. The output voltage of the inverter is fed to single-phase induction motor and analyzed the response with and without filter.

3 Simulation Results of NLC Based MLI

The proposed 17-level inverter is simulated with filter and without filter. In the existing system, the THD value of voltage is 4.87% and the output voltage is 81.27 V at the fundamental frequency of 50 Hz. In the existing system, the THD value of current is 2.09% and the output current is 8.11 A at the fundamental frequency of 50 Hz [20].

Figures 4 and 5 show the simulation output of proposed 17-level voltage and current. An imperative issue in MLI configuration is to generate sinusoidal output voltage waveform and to take out lower order harmonics as did in [4, 5].

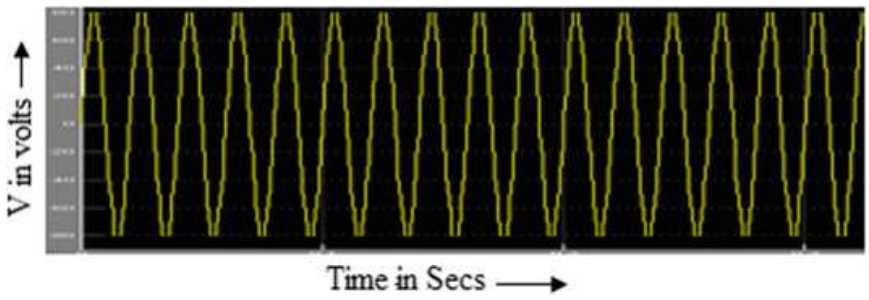

Fig. 4 Output voltage waveform of 17-level inverter

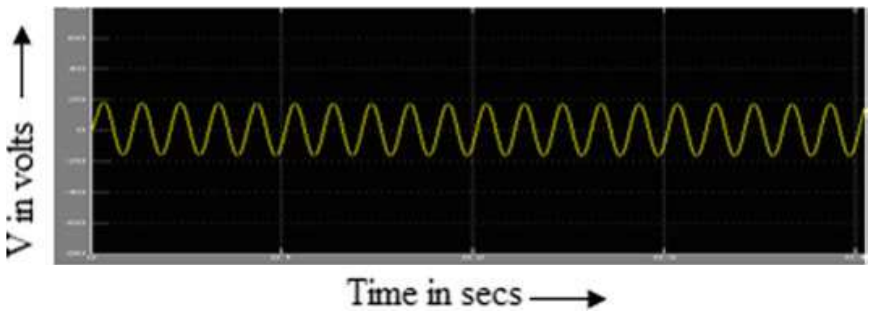

Fig. 5 Output current waveform of 17-level inverter

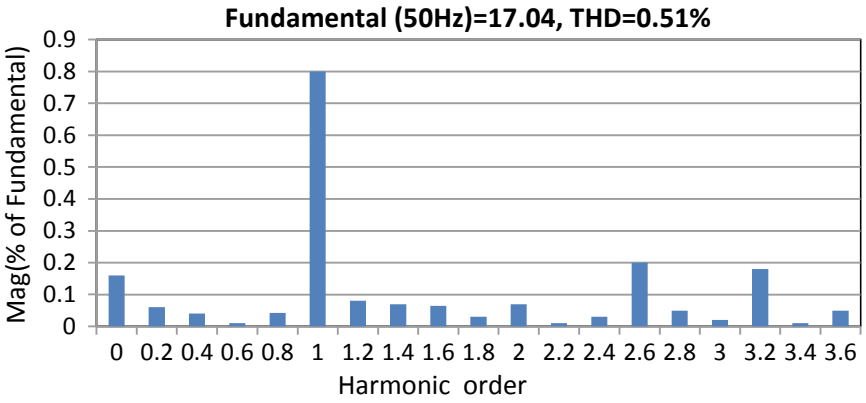

Fig. 6 FFT analysis of output current without filter

3.1 NLC Based MLI Without Filter

Figure 6 shows that the FFT harmonics spectrum is sampled with the harmonics up to 20th order. The measured output current THD is 0.51%. From the results, it's clear that proposed topology has slightly higher THD compared to topology with filter.

3.2 NLC Based MLI with Filter

Figure 7 shows the output of FFT analysis of the proposed system current with filter. From FFT analysis, the proposed system current THD without filter is 0.51% and with filter is 0.3% for the fundamental frequency of 50 Hz. From the result, it's clear that proposed topology with filter has better THD compared to topology without filter.

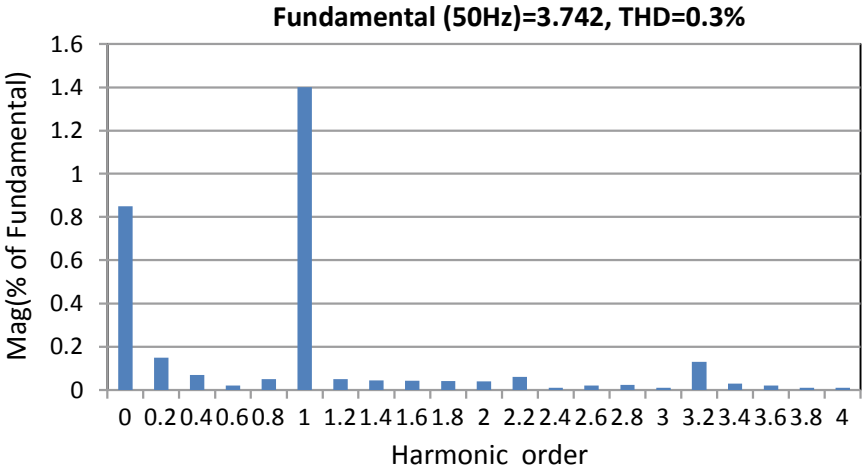

Fig. 7 FFT analysis of output current with filter

4 Experimental Setup and Analysis

The 17-level ST-type multilevel inverter fed 300 W single-phase induction motor is shown in Fig. 8. The experimental setup includes inverter circuit with 12 numbers of MOSFET (IRF540), FPGA, power supply, filter, and single-phase induction motor. FPGA controller generates sinusoidal PWM pulses. Switching pulse to the multilevel, it is generated from FPGA Controller [22, 23]. DC source is applied to inverter circuit from single-phase AC supply. The opto-coupler output signal is inverted from original PWM input signal. Load is connected across the power circuit and the output voltage and current are measured using DSO. Figures 9 and 10 show the hardware output waveform of proposed system current and voltage.

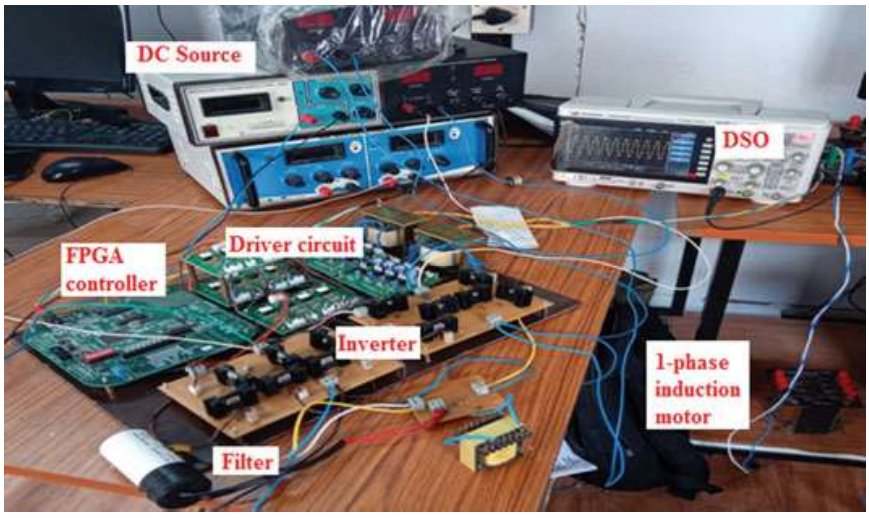

Fig. 8 Experimental setup of NLC based MLI

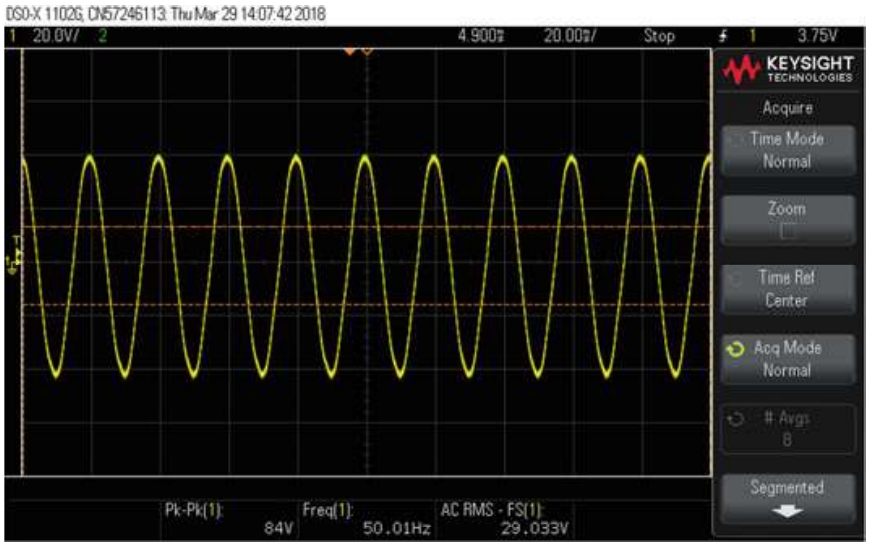

Fig. 9 Output current waveform of NLC based MLI

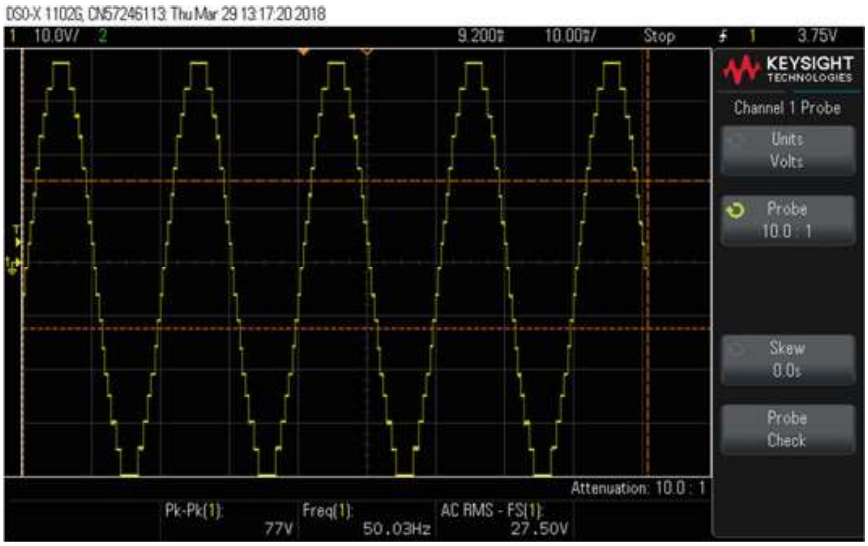

Fig. 10 Output voltage waveform of NLC based MLI

The ST-type module for NLC scheme based 17-level MLI proposed in this paper with a reduced number of switches has resulted in reduction of THD and switching losses. Based on the analysis, it is witnessed that the circuit is extremely simple compared to that of classical topologies.

5 Conclusion

This paper has presented a novel design of 17-level ST-type MLI module with reduced components using NLC Scheme. It is clear from the analysis that the proposed module can be utilized in high-voltage controlled drive applications by cascading principle. The proposed system has low switching stress on the switches which will improve the reliability of the inverter. The THD in current is very low as 0.3% with a simple LC-filter.

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