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Gayatri V ; Amirtha T ; S. Padmapriya   All Authors •••

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This paper introduces an innovative approach to enhancing Vedic multipliers using approximate full adders with 2X1 multipliexers. The study compares this novel design with traditional multipliers, highlighting its superior performance in terms of area utilization, processing speed, and power efficiency. Furthermore, the research extends the application of this design by implementing it with 4-bit approximate carry look-ahead adders, showcasing its adaptability and scalability across different bit widths. The experimental findings demonstrate the significant advantages of the proposed approach over conventional designs, establishing it as a promising solution for achieving efficient arithmetic operations in digital circuits.

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