



An Energy-Efficient Double-Tail Current-Shaped Comparator for High-Speed Low-Power SAR ADCs for ECG Filtering

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Abstract

High-speed, low- power comparators are an essential element of modern ADCs, especially for biomedical and mixed-signal VLSI systems. This work proposes a novel Double Tail comparator with Clock Shaped (DTCS) Controlled device. The DTCS achieves low-power, low-jitter operation due to the pre-amplification process. By using clocked-tail transistors, the pre-amplifier and latch stages are isolated, and early voltage gain is achieved by minimizing dynamic charge sharing among internal nodes. These improvements cumulatively reduce the energy dissipated per decision. It is designed in a 65 nm CMOS process with a supply voltage of 1.1 V. The comparator can operate at speeds up to 1 GHz and can drive a load of 10 fF. Simulations are carried out in the Cadence Virtuoso environment, and the results show a propagation delay of 120–150 ps and a power consumption of 13–18 μ W. Also, input-referred noise of 0.08 μ V RMS and a power- delay product of 2.03 fJ are reported, which outperform conventional double- tail designs. Benchmarking against recent state- of- the- art comparators, the proposed model highlights a balanced optimization of speed, power, and noise. Compared with state-of-the-art models, the DTCS achieves a 22.2% reduction in power consumption, and 11.7% reduction in delay, and a 16.11.7% reduction in leakage power. This design utility is demonstrated through an ECG acquisition as a case study. The performance is measured by Signal- to- Noise- and- Distortion Ratio (SNDR), Effective Number of Bits (ENOB), and Spurious- Free Dynamic Range (SFDR). The post- simulation results show remarkable improvements of 7% in ENOB, 12.2% in SFDR, and 9.9.4% in SNDR. Hence, the proposed work demonstrates a scalable, low-noise, and energy-efficient comparator that establishes a strong and reliable foundation for next-generation high-speed, low-power ADCs, particularly suited for biomedical signal processing and mixed-signal VLSI applications.

Extended author information available on the last page of the article

Keywords ADC: Analog-to-digital converter · DTCS: Double tail clock shaped · ECG: Electrocardiography · SNDR: Signal-to-noise-and-distortion ratio · ENOB: Effective number of bits · SFDR: Spurious-free dynamic range

Abbreviations

ADC	Analog to digital converter
ADE	Analog design environment (cadence)
AMS	Analog mixed-signal (designer)
CCCDT	Cascode cross-coupled dynamic logic comparator
CCT	Clock controlled tail
CDT	Conventional double-tail (comparator)
CMOS	Complementary metal–oxide–semiconductor
DLC	Dynamic latch comparator
DT/DTL	Double tail logic
DTC	Double tail comparator
DTCS	Double-tail current-shaped comparator (proposed design)
DyC	Dynamic comparator
DyCC	Dynamic CMOS comparator
ECG	Electrocardiography
EDA	Electronic design automation
EDP	Energy delay product
EEG	Electroencephalography
ENOB	Effective number of bits
FF	Fast–fast (process corner)
FoM	Figure of merit
ICMR	Input common mode range
IoT	Internet of things
MDT	Modified dynamic tail comparator
MIT-BIH	Massachusetts institute of technology–beth israel hospital (arrhythmia database)
NMOS	N-type metal–oxide–semiconductor
ODT	Optimized double-tail logic comparator
PDP	Power delay product
PVT	Process, voltage, temperature
QRS	QRS complex (ECG waveform feature)
RMS	Root mean square
RRDC	Rail-to-rail dynamic comparator logic
SAR	Successive approximation register
SFDR	Spurious-free dynamic range
SNDR	Signal-to-noise-and-distortion ratio
SNR	Signal-to-noise ratio
SoC	System on chip
SS	Slow–slow (process corner)
TT	Typical–typical (process corner)

VLSI	Very large scale integration
WFDB	Wave-form database (python/MATLAB toolbox)

1 Introduction

The Dynamic comparators are critical components in modern electronics and are known for their speed and high-power mixed-signal circuits. These comparators are commonly used in various Analog to Digital Converters (ADC) such as Flash, Successive Approximation Register (SAR) and Pipeline ADCs [1]. The SAR model is depicted in Fig. 1a. The character of the comparator is to rapidly switch and decide the accurate digital output values based on the provided Analog input value by the circuits. The Dynamic Comparator (DyC) is preferred over static comparators for real-time signal conversion. The DyC has high-speed, zero-static power, and follows the clock-generation mechanism for better performance [2]. However, these DyC comparators do not meet real-time requirements due to scaling constraints and power leakage, making CMOS-based DyC unsuitable for portable biomedical devices and IoT edge devices. These issues bring the researcher to work on optimization of the delay power trade-off [3]. Also, a method was proposed to minimise the secondary effects of CMOS at the subthreshold level, thereby mitigating various noise-offset kickback effects. Two CMOS logic methods that have been developed to address emerging issues are Double Tail comparators (DTC) logic and StrongARM logic. These transistor models are illustrated in Fig. 1b, c, and d.

1.1 Survey Based on Existing Methods

Certain research work suggested that the DyC achieves better accuracy with limited noise and high-speed signal regeneration, enabled by high-speed conversion at the sampling latch stages. However, the DyC are closely affected by the power consumption and delay at the regeneration units of ADC. Recent studies focused on the architectural enhancement of Double Tail Logic (DTL) by incorporating cross-coupled pre-amplifiers. The improved design of latches and common-mode optimisation is expected to enhance the accuracy.

The major focus of this research work is to fulfil the requirements of modern ADC. The clocking methods and cross-coupled method have played a pivotal role in optimising the power-delay product (PDP) and the optimisation of the power-delay trade-off. The authors of [1] and [2] address the evolution of DyC and Strong- ARM based designs mainly focusing the power, speed and noise performance. As these DyC are integral part of many ADC which are implemented in IoT and bio medical devices as specified by [3] Zhan et al. and [4] Thoutam et al.

The research work presented in [5] and [6] discussed about the recently developed ADC in-terms of power consumption and coupling of the transistors. In addition, the properly designed DyC employing DTL exhibits significantly lower propagation delay, energy consumption, and switching power compared to conventional methods.

behavioral analysis using extracted comparator characteristics such as delay, offset, jitter, and power consumption. Standard ECG input signals from the MIT-BIH Arrhythmia Database were applied to evaluate system-level signal acquisition performance. The improvements achieved at the comparator level directly contribute to enhanced ADC behavior by reducing decision latency, minimizing regeneration error, and lowering dynamic power consumption during successive approximation operations. Consequently, the proposed DTCS architecture demonstrates improved ENOB, SNDR, ECG output SNR, and QRS detection accuracy when compared with conventional comparator structures, thereby establishing a direct relationship between comparator-level optimization and overall ECG acquisition performance.

5.2 Limitation

While the proposed double-tail current-shaped comparator achieves improved energy efficiency and speed, its practical deployment in ECG-based SAR ADC systems faces certain constraints. The design is sensitive to PVT variations, leading to offset and timing inaccuracies that can affect low-amplitude ECG signal integrity. Dynamic switching operation introduces kickback noise and leakage effects, which may distort biomedical signals without careful front-end conditioning. Additionally, precise current shaping increases design and layout complexity in scaled technologies. The comparator also relies on stable clocking, making it vulnerable to jitter. Hence, additional calibration, filtering, and noise mitigation techniques are often required for reliable real-time ECG acquisition.

6 Conclusion

This work presents a novel double-tail comparator architecture with cross-coupled pre-amplification. This research focuses on optimising the DTCS for low power, low delay, and reduced noise, making it suitable for modern high-speed VLSI applications in mixed-signal and biomedical signal processing. Through extensive simulation in a 65 nm CMOS process, the proposed design demonstrates significant improvements over conventional and recent literature comparators: propagation delay reduced to 120–150 ps, power consumption lowered to 13–18 μ W, and input-referred noise minimized to 0.8 μ V RMS. The power–delay product of 2.03 fJ highlights its energy efficiency, making it highly suitable for low-power, high-speed ADC applications. Benchmarking against various state-of-the-art comparators shows that the proposed design achieves a balanced optimisation of speed, power, and noise, and could outperform both conventional double-tail and advanced StrongARM and rail-to-rail designs. The design's robustness across input voltage variations and frequencies up to 1 GHz ensures high reliability in mixed-signal VLSI systems. The ECG signal case study demonstrates practical relevance, showing that the comparator can accurately digitise microvolt-level biomedical signals in wearable or portable monitoring devices while consuming minimal energy. This method shows the feasibility of deploying the proposed architecture in real-world low-power, high-precision biomedical systems. This

framework offers a compelling solution for next-generation ADCs in both biomedical and high-speed VLSI applications.

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Author Contributions

Dinesh Kumar Jayaraman Rajendiran (Corresponding Author) conceptualized the research framework, developed the double-tail current-shaped comparator architecture, formulated the unified power delay optimization strategy, supervised the experimental simulations, and coordinated manuscript preparation and revisions. Priyadharsini K contributed to the optimization methodology, implementing and validating the proposed framework against conventional comparator designs, and assisted in the results and discussion sections. Ganesh Babu C was responsible for circuit modelling, simulation setup, performance analysis across process corners, and preparation of comparative tables and figures. Karthi S P supported the implementation of transient and static simulation routines, aided in benchmarking against existing low-power comparator architectures, refined the literature survey, and contributed to manuscript writing and presentation of results.

Data Availability The code part is available for this work, and if required, the results can be shared.

Declarations

Conflict of interest We hereby declare that NO affiliations involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript. This manuscript work was solely done by the author under the guidelines of the supervisor Dr. C. Ganeshbabu.

Consent to participate The authors at this moment assure that this research does not involve any human participants or animals.

Ethical approval This research did not involve human participants, animals, or any form of clinical experimentation. The ECG dataset employed in this study was obtained from publicly available benchmark repositories and used strictly in compliance with the terms and conditions of the source. The usage of AI tools used for the illustrations as per the authorized services. Therefore, ethical approval and informed consent were not required.

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