

Power-Efficient Multiplier: Leveraging Approximate Designs and Modified Gate Diffusion Technique

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Abstract— In today's modern market, the demand for efficient computational blocks that can execute complex operations with minimal power consumption is ever-increasing. One of the critical components in these computational blocks is the multiplier circuit, which directly impacts the performance of the overall system. To address this need, researchers are continuously striving to optimize multiplier circuits in terms of speed, power, and area requirements. This idea aims to optimize multiplier circuitry through experimental analysis, focusing on parameters such as propagation delay, power consumption, area, and power-delay-product (PDP) using Cadence Virtuoso. Low power consumption is a crucial requirement in CMOS integrated circuit design, and recent research suggests that implementing approximate designs can achieve this goal more effectively than accurate designs. In multimedia applications, Digital Signal Processing (DSP) blocks play a vital role, particularly in video and image processing algorithms. As the human perception of these outputs allows for numerical approximation, there's an opportunity to leverage approximate analysis to achieve further optimization. In this work, we propose the utilization of approximate multipliers to meet these demands. By leveraging these techniques, we aim to contribute to the advancement of low-power, high-performance computational blocks, meeting the evolving needs of modern markets.

Keywords—MDGI, VLSI, approximate multiplier.

I. INTRODUCTION

Digital Signal Processing (DSP) applications, particularly those involving multimedia outputs like images for human recognition, demand efficient processing solutions that balance accuracy with power consumption. Traditional arithmetic circuits, such as adders and multipliers, form the backbone of DSP processors [2]. However, their exact operations often lead to significant power consumption and performance lags. In order to address these challenges, approximate arithmetic circuits have emerged as a promising solution. By relaxing accuracy constraints, approximate circuits offer opportunities for significant power savings and performance enhancements. In DSP applications where human perception tolerates certain inaccuracies, leveraging approximate arithmetic becomes particularly advantageous.

In our proposed approach, we leverage the modified gate diffusion technique to further optimize power consumption in our approximate multiplier circuitry. This technique involves the utilization of reduced transistor layouts, specifically Gate Diffusion Input (GDI) and Modified GDI (Mod-GDI), which have demonstrated significant potential in mitigating power

dissipation while maintaining circuit performance [6]. While GDI has shown promise in reducing power consumption, it has certain limitations, including challenges in addressing bulk terminal bias and achieving optimal performance levels. To overcome these limitations, we integrate Mod-GDI technology into our design. Mod-GDI enhances the efficiency of transistor utilization, allowing for more precise control over power consumption without compromising circuit performance. By implementing this modified diffusion technique in our approximate multiplier, we aim to further enhance its power efficiency, thereby enabling high-performance DSP applications with reduced energy overheads. This innovative approach not only minimizes power consumption but also contributes to the overall optimization of our proposed circuit design, ensuring efficient operation without sacrificing performance metrics critical for DSP applications.

II. LITERATURE SURVEY

Cong Liu, et al. presented an innovative approximate multiplier for error-tolerant applications like DSP, utilizing a novel approximate adder to minimize carry propagation. Configurable error recovery enables varying levels of accuracy. Simulations on a 16-bit multiplier in a 28nm CMOS process demonstrate a 20% delay reduction and up to 69% power savings compared to a Wallace multiplier. The proposed design offers comparable accuracy to exact multipliers but with significantly improved power efficiency and performance, achieved through a shorter critical path and configurable error recovery. Gondh Navabharat Reddy proposed an approach to low-power integrated circuit design using approximate designs in CMOS technology. It proposes PA1 and PA2 approximate adders, a 4-2 compressor, and an approximate 4x4 multiplier, achieving significant reductions in delay and power consumption compared to accurate designs. Simulations conducted in 90nm technology validate the efficacy of the proposed designs, which are particularly suitable for multimedia applications where numerical exactness is not critical. Parag Kulkarni, et al. proposed a multiplier architecture with tunable error characteristics, offering significant power savings of 31.78% to 45.4% over accurate designs, with an error range of 1.39% to 3.32%. Through sample applications like image filtering and JPEG compression, it demonstrates 2X to 8X better Signal-to-Noise Ratio (SNR) compared to voltage over-scaling methods. The architecture's benefits vary depending on design size and application. It introduces a circuit-centric approach for power-quality trade-offs and proposes a correction mechanism for

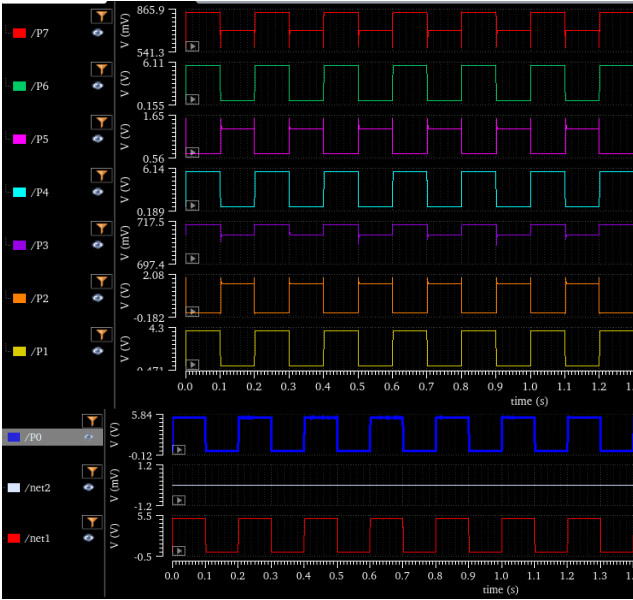


Fig 12. Transient response of the 4*4 Multiplier

TABLE III. ERROR TABLE FOR APPROXIMATE 4*4 MULTIPLIER

A [3:0]	B [3:0]	Accurate Product	Appo. Product	Error Distance (ED)
0000	0000	00000000	00001110	3
0101	0111	00100011	00101110	3
1111	1111	11100001	11100111	2
1111	1011	10111101	10110011	3
1011	1001	01100011	01101101	3
1010	1101	10000010	10001111	3
1110	1101	10100100	10100010	2
0110	1000	01110010	01111110	2
0100	1000	01000000	01001110	3
0001	0100	00000010	00000110	1

E. Error Metric – Error Distance (ED)

To evaluate the accuracy of the proposed approximate multiplier, the Error Distance (ED) metric is used. ED is defined as the absolute difference between the correct output and the approximate output:

$$ED = | \text{Exact Result} - \text{Approximate Result} |$$

This metric provides insight into the extent of deviation introduced by approximation. Since errors in low-significance bits (LSBs) may have less visual or functional impact in DSP applications, ED helps assess the trade-off between power savings and computational accuracy.

IV. RESULTS AND DISCUSSION

Analysis of the implemented approximation-based multiplier architecture, incorporating Modified Gate Diffusion Input (MGDI) techniques, showcase notable improvements in error management and performance metrics. The computed Error Distance (ED) values for various input combinations were used to assess the approximation quality. As shown in Table III, most errors

occur in the least significant bits (LSBs), resulting in small ED values. The maximum ED observed was 3, and the average ED was 2.5, confirming that the proposed design introduces controlled and predictable errors. Leveraging MGDI in the circuitry design contributes to significant reductions in transistor count and power consumption, enhancing overall efficiency. Through comprehensive error analysis, it is observed that the MGDI-based approximate multiplier effectively mitigates errors, particularly in the least significant bits (LSBs), ensuring reliable operation. Error Distance (ED) calculations highlight the accuracy of the approximate multiplier design, demonstrating minimal deviations from accurate arithmetic operations.

Table IV, illustrates a comparison between the approximate multiplier implemented using the Modified Gate Diffusion Input (MGDI) technique and the transmission gate-based design [2].

TABLE IV. THE POWER AND THE DELAY ANALYSIS OF THE APPROXIMATE MULTIPLIER AND ITS UNITS.

Design	Power (μ W)	Delay (nS)	PDP (fj)
Approximate Multiplier (Old)	29.332	124.56	3653.59392
Approximate Multiplier (MGDI)	0.7696	31.57	24.296272
PA1 (Old)	1.13	0.755	0.85315
PA1 (MGDI)	0.224	0.1039	0.023274
Half Adder (MGDI)	2.633	0.06138	0.161614
Compressor (Proposed)	1.06	87.36	92.6016
Compressor (MGDI)	0.4514	4.76404	2.150488
AND Gate (MGDI)	0.1851	0.02906	0.005379

V. CONCLUSION

From literature, we are able to see that implementing approximate multiplier using MGDI method the power consumption is reduced and the delay reduced significantly. By collecting data from our references, we can see that, power consumed is 29.32 micro-Watt and delay is 124.56 nano seconds by normal implementation of approximate circuits without optimization [2]. But by MGDI design style, the power consumed is 0.7696 micro-Watt and the delay is 31.57 nano seconds. When we compare the results, we can conclude that by MGDI design style the power consumption and delay has decreased. Thus, an efficient multiplier is designed by using above design.

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