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ORIGINAL ARTICLE

Efficient compression methods using combining the code based encoding techniques

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Abstract The two main problems with testing integrated chips of the current generation are testing power and testing expense. Test data amount and transmission time are connected to testing costs. In addition to increasing memory needs, larger data volumes also result in longer testing times. In scan-based test applications, several effective test data compression methods are suggested to reduce test time and test data volume at the same time. To improve the compression ratio, the test data is compressed using a combination of the compatible block coding and Huffman coding technique is first proposed method. Second proposed method is Hamming coding, Bitmask dictionary, and the 2nPattern Run Length coding algorithm were combined to create hamming coding and BDPRLC, which compresses test data in order to increase the compression ratio. A decompression algorithm was implemented using VHDL program. MATLAB code was used to implement compression method, and the compression ratio for different circuits was assessed using test vectors of benchmark circuits, ISCAS 89.

Keywords Compression · Huffman · Compatible · Hamming · 2^n PRL · Hybrid

1 Introduction

In addition to requiring a large volume of test data to test and validate the intellectual property (IP) cores of System-On-Chip design, modern CMOS circuits integrate millions of transistors into a single chip, increasing manufacturing defects. These chips must be physically tested using various patterns as input (test vectors), which are generated by a pattern generator. During test application, these massive test sets are placed in Automatic Test Equipment (ATE), which has insufficient memory, I/O pins, and bandwidth. It is preferable to compress the test data before transferring it to the ATE, which reduces test time and testing expense.

Testing shows that the power dissipation is carefully exceptional in relation to normal mode. Because of the low associated test vectors used during testing, the logic state transitions occur more frequently. The needless power dissipation at circuit nodes is caused by this fake transition. The circuit becomes operationally impaired due to the excessive scan-shift powers. The good circuit may be compromised by the increased yield loss caused by the high peak power. The primary source of warmth is peak power, which raises the price of the cooling package (Abramovici et al. 1990). Application-aware bitmask and dictionary selection algorithms were employed in efficient code compression

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techniques to increase code compression effectiveness without adding any overhead associated with decompression. An effective test compression method based on block merging was presented (El-Maleh 2008). Numerous compression coding algorithms have been developed in the literature because testing System-on-a-Chip (SoC) is becoming increasingly difficult due to the massive number of test data. One useful technique for cutting down on test data volume and testing time is test data compression. By combining the improved performance of various techniques, the low power testing survey may be utilised to test VLSI circuits using compression methods (Kalamani et al. 2013). The Block Merging (BM) compression technique is based on partitioning the test set into blocks of size b bits and then merging consecutive compatible blocks. Two blocks are considered compatible (Bin et al. 2013). Run length encoding and bit mask-based data compression were proposed (Jagadeesh et al. 2012). The technique put forthmakes use of precisely nine code words. A block of data can be represented as 0 (all zeros), 1 (all ones), or U (mixed 0, 1, and don't-care bits) to indicate that it is identical or not in the nine-coded compression (9C) technique (Tehranipoor et al. 2005). In addition to requiring more memory, larger test data sets also require more testing time. Several methods have been suggested in the past to reduce the amount of test data and test time in scan circuits, and the majority of these use compression to do this. In a straightforward compression method, the number of flip-flops per scan chain is decreased, increasing the number of scan chains in the circuit. As a result, the test time is decreased overall because less time is required to shift the input vector bits through scan flip-flop. The paper is structured as follows. The paper is organized as Sect. 2 discusses the existing approaches and Sect. 3 describes the proposed methods. Section 4 describes the results and discussion and concluded in Sect. 5.

Table 1 Generation of Compatible block code

Number of Data block	Sign bit	Compatible Code word	Sign bit	Compatible Code word
1	0	001	1	000
2	0	010	1	010
3	0	011	1	011
4	0	100	1	100
5	0	101	1	101
6	0	110	1	110
7	0	111	1	111
8	0	000	1	000

2 Existing method

These tactics work well for correlation-related activities, despite the more complex control logic. The researchers can examine the possibility of combining the various methods for additional compression, taking into consideration the area overhead of the on-chip decoder as well as the overall test time, test volume, and test power. The difference vector has been identified using the pre-computed test set by the Golomb coding (Chandra and Chakrabarty 2001). To improve the compression ratio, a Mixed Selected Selective Huffman Coding and Run Length Coding algorithm was created by combining Selected Selective Huffman and Run Length coding. Compatible block coding can be used to encode test data blocks that are complementary and inversely compatible. Thus, the run length strategy enhances the compression ratio and reduces the massive data volume. Multilevel Huffman coding (Kavousianos et al. 2007) recommends a combination of run length and huffman coding. In order to determine the frequency directed run length codes, the approach employed to find the number of runs of zeros in the test vectors is ineffective if there are a lot of mixed ones and zeros. methods including equal-run-length coding (ERLC) coding (Maleh 2008), Alternating variable-length (AVR) coding (Ye et al. 2011), and alternate FDR

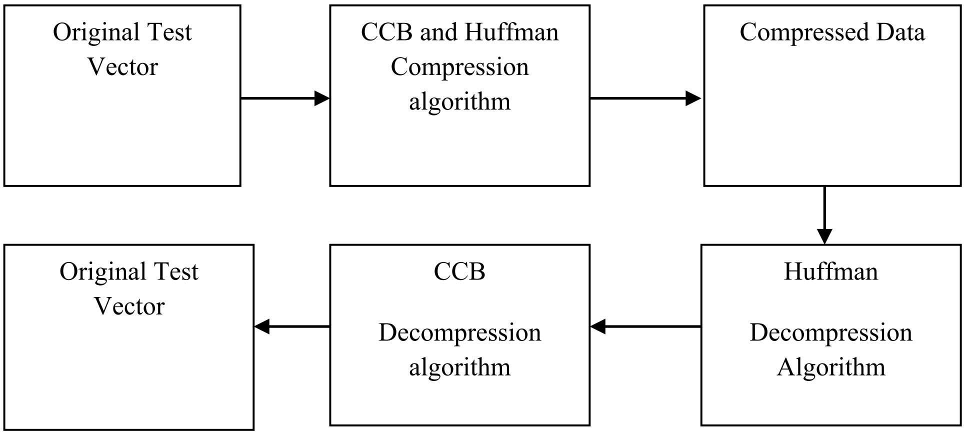

Fig. 1 Block Diagram of Test Data Compression/Decompression Method of Combined Compatible Block and Huffman Coding

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Declarations

Conflict of interest There is no conflict of interest.

Human participants and/or animals This article does not contain any studies involving animals performed and any studies involving human participants performed by any of the authors.

Informed consent Not applicable as no human or animal sample was involved in this study.

References

Abramovici M, Breuer MA, Friedman AD (1990) Digital system testing and testable design. IEEE press, The Institute of EEE Inc

Azar J, Makhoul A, Couturier R, Demerjian J (2020) Robust IoT time series classification with data compression and deep learning. Neurocomputing 39(8):222–234

Chandra A, Chakrabarty K (2001) System-on-a-chip data compression and decompression architecture based on Golomb codes. IEEE Trans Comput- Aided des Integr Circuits Syst 20(3):355–368

Chen GY (2021) New variable-length data compression scheme for solution representation of meta-heuristics. Comput Oper Res 131:105256

Chowdhury MR, Tripathi S, De S (2020) Adaptive multivariate data compression in smart metering internet of things. IEEE Trans Industr Inf 17(2):1287–1297

El-Maleh AH (2008) Efficient test compression technique based on block merging. IET Comput Digital Tech 2(5):155–163

Jagadeesh S, Venkateswarlu T, Ashok M (2012) Run length encoding and bit mask based data compression and decompression using verilog. Int J Eng Res Technol (IJERT) 11(7):1–7

Jha CK, Kolekar MH (2021) Empirical mode decomposition and wavelet transform based ECG data compression scheme. Irbm 42(1):65–72

Jin S, Zhang L (2013) Test data compression scheme based on compatible data block coding. Inf Technol J 12(1):204–208

Kalamani C, Paramasivam K (2013) Survey of low power testing using compression techniques. Int J Electron Commun Technol 4(4):13–18

Kavousianos X, Kalligeros E, Nikolos D (2007) Multilevel Huffman coding: an efficient test-data compression method for IP cores. IEEE Trans Comput Aided Design Integr Circuits Syst 26(6):1070–1083

Lee L-J, Tseng W-D, Lin R-B, Chang C-H (2012) 2^n pattern run-length for test data compression. IEEE Trans Comput Aided Design Integr Circuits Syst 31(4):644–648

Lee J, Yoon S, Hwang E (2021) Frequency selective auto-encoder for smart meter data compression. Sensors 21(4):1521

Maleh AH (2008) Test data compression for system-on-a-chip using extended frequency-directed run-length code. IET Comput Digital Tech 2(3):155–163

Shukla NK, Mayet AM, Raja MR et al (2024) A unified test data volume compression scheme for circular scan architecture using hosted cuckoo optimization. J Supercomput 80:6411–6434

Sivanantham S, Mallick PS, Perinbam RP (2014) Low-power selective pattern compression for scan-based test applications. Comput Electr Eng 40(1):1053–1063

Tehranipoor M, Nourani M, Chakrabarty K (2005) Nine-coded compression technique for testing embedded cores in SOCs. IEEE Trans Very Large Scale Integr (VLSI) Syst 13(6):719–731

Wu TB, Liu HZ, Liu PX (2013) Efficient test compression technique for SoC based on block merging and eight coding. J Electron Test: Theory Appl 29(6):849–859

Ye B, Zhao Q, Zhou D, Wang X, Luo M (2011) Test data compression using alternating variable run-length code. Integr VLSI J 44(2):103–110

Zhan W, El-Maleh A (2012) A new scheme of test data compression based on equal- run-length coding (ERLC). Integr VLSI J 45(1):91–98