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A low-power, full-custom design of a 4:2 compressor using 32 nm CNTFET technology for high-speed signal processing

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Abstract
Multiplication is a vital function in most Digital Signal Processing (DSP) applications. In general, multipliers take-up more space, have longer latency, and use more energy than other types of digital circuits. This paper will discuss the design of compressors and performance comparisons with respect to size, power, and speed. Compressors are the essential parts of multipliers that allow for the parallel accumulation and reduction of incomplete product stages. Enhancing the compressor's performance has an impact on the multiplier's capacity, which has an impact on the DSP's effectiveness. The Carbon Nanotube Field Effect Transistor (CNTFET) has benefited from the Fin Field-Effect Transistor (FinFET) because carbon nanotubes are the stiffest and sturdiest materials. Due to its superior regularization and reduced complexity, the compressor structure is generally selected among the other varieties. Partial product terms are condensed using a compressor into two operands in Partial Product Reduction (PPR). A new design for a compressor is proposed and tested. The performance of this new compressor is simulated and checked to that of existing ones using Cadence's Virtuoso tool, with 32 nm CNTFET technology. Simulation outcomes confirm that the projected compressor reduces delay by 10.31%, EDP by 30.82%, and PDP by 25.09%, outperforming existing ones.

Keywords CNTFET · Compressor · Low power · High speed · Monte Carlo

1 Introduction

The technique of entrenching lots of transistors on a sole silicon microchip is referred to as Very Large Scale Integration (VLSI) [1]. Based on the number of transistors packed inside the semiconductor integrated circuit, VLSI emerged from small-scale integration (SSI). The research strategy is to design new low-power systems using precise and effective power estimation techniques. VLSI enables the integration of all of these components into a chip [2]. By occupying less space, accelerating operations, consuming less power, and costing less money, VLSI technology decreases circuit size. To design integrated circuits, VLSI uses system-on-a-chip architecture [3].

With remarkable electrical features like high carrier mobility, ballistic transport, and better electrostatic control CNTFETs are new nano electronic devices that use semiconducting carbon nanotubes as the channel material rather than silicon. Compared to conventional MOSFETs, these characteristics allow CNTFETs to produce higher ON current, lower OFF current, and improved scalability, particularly with low nm technologies [4, 5]. The precise control of nanotube chirality (to guarantee semiconducting behaviour), the alignment and placement of CNTs on a wafer, and the lowering of contact resistance are the main obstacles to CNTFET production, notwithstanding its benefits. With minimal changes, CNTFETs can be integrated into current semiconductor production workflows because they are generally compatible with CMOS processes. This compatibility and their excellent performance characteristics make

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CNTFETs a promising option for extending Moore's law and opening the door to next-generation high-speed, low-power devices [4].

In terms of energy efficiency and fewer short-channel effects, CNTFETs perform better than FinFETs and nanowire FETs. A carbon nanotube or an array of carbon nanotubes is used as the substrate in the channel of a CNTFET, as opposed to a standard MOSFET. CNTFETs' performance characteristics are different from MOSFETs' [6, 7]. The channel uses a small portion of the heat generated in the CNTFET. The bandgap of a carbon nanotube is directly related to the CNTFET's chiral angle and diameter. Carbon nanotubes may be the ideal candidate for next-generation nanoscale transistor devices if such features can be implemented [8]. Theoretically, carbon nanotubes can transport heat almost as well as diamond or sapphire, and because of their small size, CNTFETs should switch reliably while consuming far less power than silicon-based devices. Modern solutions exist to address these concerns in accordance with Moore's law [9].

DSP devices are the most important component of rechargeable battery portable computers due to their high circuitry, better performance, and reduced power consumption, making them an excellent computing platform for multimedia applications and image processing applications [10]. The multiplier is a crucial component of the DSP system's arithmetic block [11]. A multiplier typically consists of three stages: Partial Product Generation (PPG), in which the multiplier and multiplicand bits are ANDed to create the partial product operands. In Partial Product Reduction, the 4:2 compressor is used in this stage to condense partial product terms into two operands. In Carry Propagating Addition (CPA), the result is obtained by adding the two operands together in this stage [12–14].

In the 4:2 compressor (existing model 1), deuce complete conventional full adders are combined in cascade style to create a compressor, as in Fig. 4. Four binary inputs plus a carry from a less important location is sent to a 4:2 compressor [15]. By creating the primary carry and sum bits (carry, sum, as well as carry to the next binary position), carry-free compression is accomplished using this technique [16, 17].

In the compressor using pseudo-half adder circuitry (the existing Model 2), one full adder, two pseudo-half adders (HA+), and a 2-input NOR gate were used to create a 4:2 compressor [18]. Compared to the typical 4:2 compressor, this topology substitutes two pseudo-half adders and a 2-input NOR gate for one full adder. In contrast to the traditional compressors, this circuit design uses two pseudo-HA+ in place of one full adder and a NOR gate [19].

In the existing Model 3, a compressor was developed employing a majority gate and 4 XOR gates. This structure was created using the conventional 4:2 compressor's standard cascading of complete adders. In contrast to the traditional architecture, the entire adder's Boolean functions are translated into 3-input majority gates and 2-input XOR gates [20].

Finding the final negative signal in the partial product row is the first step in designing the new 4:2 compressor. This negative signal is subsequently reduced or eliminated using a unique technique, which aids in lowering design delay overall. This modification is incorporated into the 4:2 compressor's logical circuit. Five NAND gates, two XNOR gates, an OR gate, an XOR gate, an inverter, and a 2×1 multiplexer are all used in the design. Following circuit modification, simulations are run to assess the performance of the design, specifically with regard to transistor usage, power dissipation, and latency. Ultimately, the outcomes are contrasted with current models to confirm gains in performance indicators.

The paper then goes on to say: Sect. 2 describes the fundamental 4:2 compressor design and relevant literature-based models. The proposed model and its analysis are described in depth in Sect. 3. Using simulation and synthesis results, Sect. 4 examines the efficiency of the suggested models in comparison to their most recent incarnations. Conclusions and potential future directions are then examined.

2 Existing design and its methodologies

2.1 Traditional 4:2 compressor design using two full adders

Two complete full adder circuits were used in the design of the traditional 4:2 compressor [21]. Four binary inputs (xi) plus a carry from a less significant bit is transmitted to a 4:2 compressor [22]. With this method, carry-free compression is achieved by generating the primary carry and sum bits (Carry, Sum), as well as carrying to the next binary position (Cout).The output from the 4:2 compressor is given in the Eq. 1,

$$\text{Cout} = \text{Majority}\ [\,\text{x1} + \text{x2} + \text{x3}] \tag{1}$$

Figure 1 depicts the compressor's structure, which consists of two complete full adders. The cascade connection between the two complete adders is used. The 4:2 compressor circuit consists of four inputs ($\times 1, \times 2, \times 3$, and $\times 4$) and two outputs (sum and carry). Cout acts as Cin for the next, more important block. Cin and Cout are separate from one another and given in Eqs. 2 and 3. This attests to the compressor's carry-free operation. There are 56 transistors in this existing model.

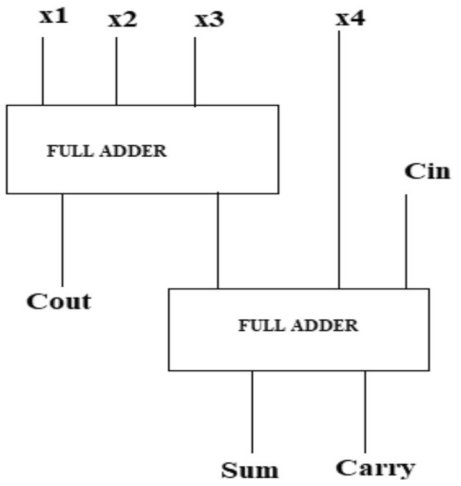


Fig. 1 Representation of 4:2 compressor using two full adders

$$\text{Sum} = \text{x1} \oplus \text{x2} \oplus \text{x3} \oplus \text{x4} \oplus \text{Cin} \tag{2}$$

$$\text{Carry} = \text{Majority}\ [(\text{x1} \oplus \text{x2} \oplus \text{x3}),\ \text{x4},\ \text{Cin}] \tag{3}$$

2.2 Compressor design using two pseudo half adders

The compressor in this current model was built using a pseudo half adder, full adder, and a NOR gate. The designed compressor structure is shown in Fig. 2. Contrast to the conventional compressor, this design replaces a full adder with two HA+and a NOR gate. Since (4:2) compressors allow regularity in VLSI systems, they have garnered more interest due to the 2:1 reduction compressor [23]. Additionally, in the place of RBAs, which use a binary-signed digit number system to represent partial products, RBAs have been used in parallel binary multiplication designs and can be more efficiently implemented by introducing a few NOT gates to 4:2 compressors. Additionally, by adopting inverted megabit encoding, the NOT gates may be removed, allowing RBAs to simply be changed out for 4:2 compressors.

In CMOS logic, NOR gates are utilized in place of XORs since they have a shorter delay. By utilizing the required carry full adder, it is possible to create NOR-based 4:2 compressor structures methodically. The pseudo-half adder circuit uses an OR gate for the carry and an XNOR gate for the sum [24, 25].

2.3 4:2 Compressor design using three input majority gate

The energy-delay trade-offs and circuit implementation methods become crucial. Designing an energy-efficient parallel multiplier necessitates investigating multiplication algorithms, technological limitations, and circuit implementation methods. The use of logic in the designs boosts the energy efficiency and dependability of circuits as compared to XOR techniques [26]. Additionally, the use of XOR logic gates and AND, OR, in new technologies that are based on the majority results in a substantial performance reduction.

The AND operation is the most basic method of partial product production. At the expense of more intricate partial product production, the Booth algorithm has been utilized to minimize partial products. The Booth approach is also used to create the negative partial products, which need two sign

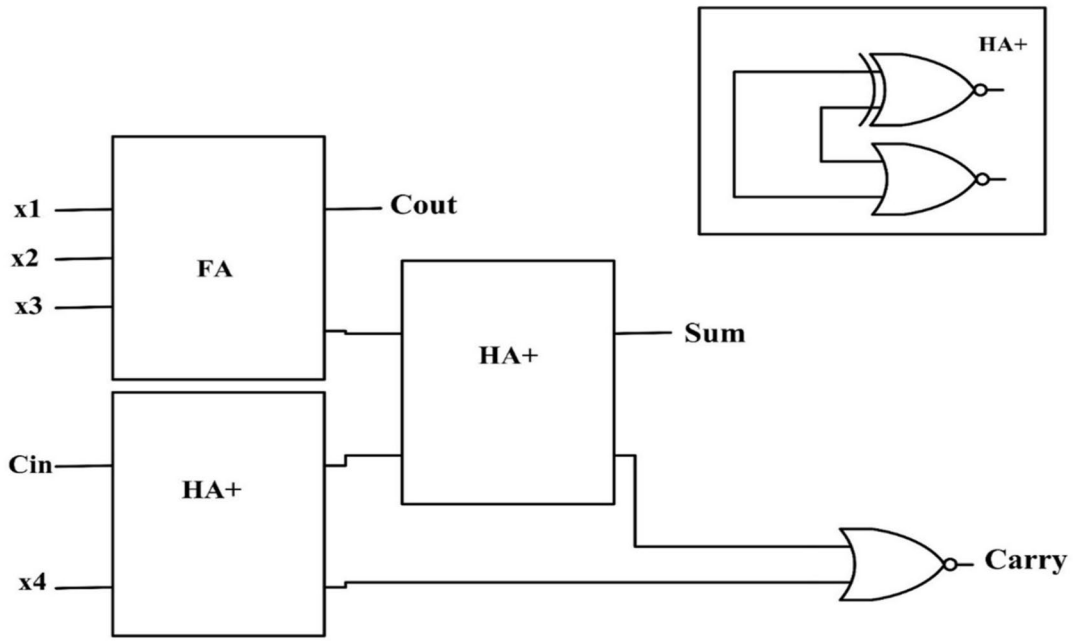


Fig. 2 Representation of 4:2 compressor using pseudo half adders

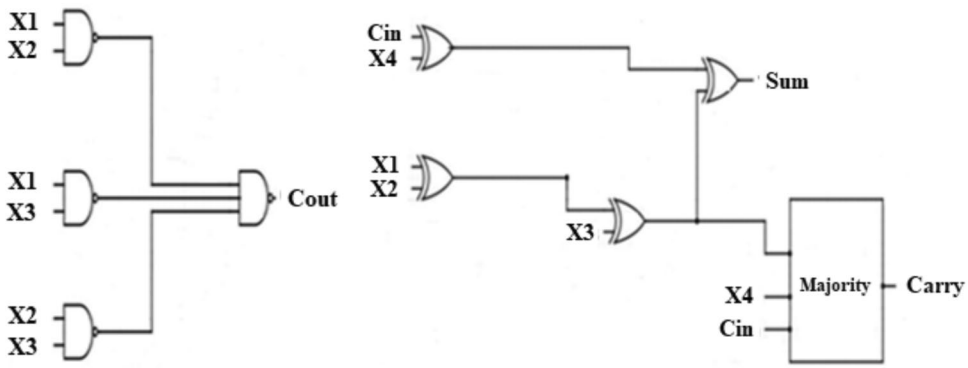


Fig. 3 Representation of 4:2 compressor using three input majority gate

bits to work properly. The second-stage PPR and other proposals to accelerate this step have been made over time. The quantity of partial products has an inverse relationship with the latency of an array multiplier. There are 48 transistors in this existing model. Delay may also be decreased with higher directive compressors. Further delay reduction can be achieved via the three-dimensional optimization method, which links quick output to delayed input.

Figure 3 shows the representation of a 4:2 compressor using a three-input majority gate [27]. The output of a majority gate is true if either of the 2 inputs are true, and the 3 inputs are given equal weight. This design makes it possible to compare any two domain relationships to those of a majority gate's inputs [28]. A complete joint will be exposed and a true output will be produced if two or more protection strands are moved; if none or just one is moved, no complete joint will be revealed and a false output will be produced. A three input majority gate is defined by the logic function is given in the Eq. 4,

$$M\ (j,\ k,\ l) = j * k + k * l + l * j \tag{4}$$

In this section, the compressors were designed using the Cadence Virtuoso EDA tool. The first existing model was designed using two efficient half adders. The second existing method was designed using pseudo-half adders along with a full adder. The third existing model is designed using a three-input majority gate [29].

3 Proposed design

This segment deals with the standard 4:2 compressor, which is designed. The study clarifies the fundamental ideas and procedures of binary multiplication as well as the problems with multipliers excessive power consumption. To create the design, a novel algorithm that lowers the last negative signal in the partial product row is discussed. A comparison of power performance is displayed.

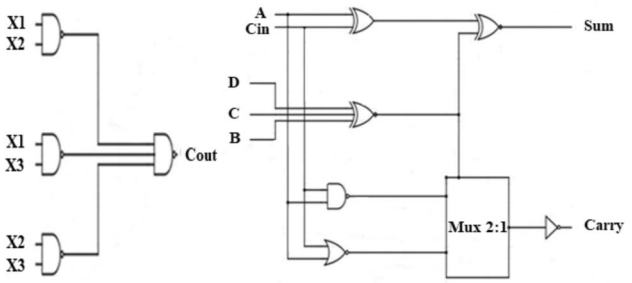


Fig. 4 Schematic view of proposed 4:2 compressor

Figure 4 shows the proposed model. The output table for the proposed 4:2 compressor at 0.9 V using a CNTFET is shown in Table 1. There are 56 transistors used in this model for the outputs Sum and Carry.

The 32 nm CNTFET design precisely optimises the use of extra logic gates, such as NAND and XNOR, with no effect on space or complexity. However, because of CNTFETs' fast carrier mobility and superior electrostatic control, power and latency reductions are substantial.

The tool view of projected compressor is shown in the Fig. 5. The equation for Sum, Carry and Cout is shown in the Eqs. 5, 6, 7,

$$\text{Sum} = (A \oplus \text{Cin}) \odot (D \odot C \odot B) \tag{5}$$

$$\begin{aligned}\text{Carry} = &\left(\overline{D \odot C \odot B}\right) . \left(\overline{A + \text{Cin}}\right) \\ &+ (D \odot C \odot B) . \left(\overline{A . \text{Cin}}\right)\end{aligned} \tag{6}$$

$$\text{Cout} = \left(\overline{\left(\overline{B . C}\right) . \left(\overline{B . D}\right) . \left(\overline{C . D}\right)}\right) \tag{7}$$

A multiplexer is a type of combinational circuit with 2n inputs and 1 output. As there are n number of selection lines, there will be 2n possible zero and one combinations [30]. The 2 × 1 multiplexer used in this proposed paradigm is just one of the various varieties of multiplexers that are currently available. For a single 2 × 1 multiplexer, there are two inputs (D0, D1), a single selection line (S), and a single output (Y). The equation for 2 × 1 Multiplexer is shown in the Eq. 8,

Table 1 Truth table of the proposed 4:2 compressor at 0.9 V

A	B	C	D	Cin	Sum	Carry	Cout
0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0
0	0	0	1	0	1	0	0
0	0	0	1	1	0	1	0
0	0	1	0	0	1	0	0
0	0	1	0	1	0	1	0
0	0	1	1	0	0	0	1
0	0	1	1	1	1	0	1
0	1	0	0	0	1	0	0
0	1	0	0	1	0	1	0
0	1	0	1	0	0	0	1
0	1	0	1	1	1	0	1
0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	0	1	1
1	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	1	0
1	0	1	0	0	0	1	0
1	0	1	0	1	1	1	0
1	0	1	1	0	1	0	1
1	0	1	1	1	0	0	1
1	1	0	0	0	0	1	0
1	1	0	0	1	1	1	0
1	1	0	1	0	1	0	1
1	1	0	1	1	0	0	1
1	1	1	0	0	1	0	1
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1	1	1	1	0	0	1	1
1	1	1	1	1	1	1	1

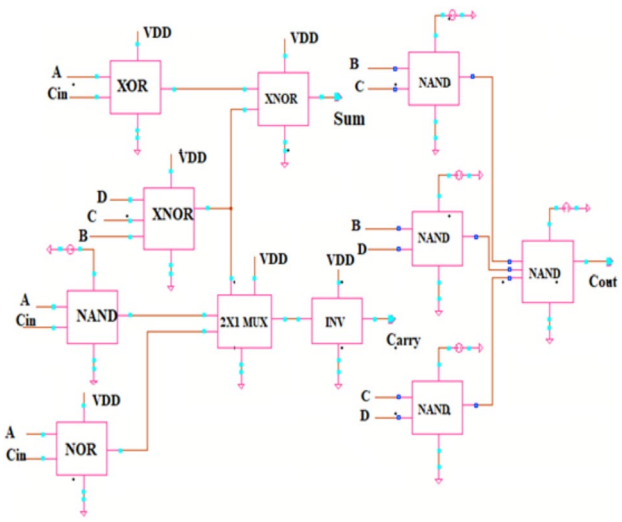


Fig. 5 Tool view of proposed 4:2 compressor

$$Y = D_0.S + D_1.S \tag{8}$$

An effective 4:2 compressor model is created in this research paper and executed with the use of an efficient 2×1 multiplexer instead of a three input majority gate. The four inputs A, B, C, D, and Cin are routed through the basic logic gates, and the outputs Sum, Carry, and Cout are obtained. The analysis was done for various voltages. The voltage values range from 0.7 V to 1.1 V. The four NAND gates were used to get the output Cout. The use of a 2×1 multiplexer in place of a majority gate reduces power and delays. The output from the multiplexer is given to the inverter in order to get the output Carry.

4 Results and discussion

The design and simulation of the existing and proposed methods are designed using Cadence software. The delay, dynamic power, EDP, and PDP for the existing and proposed

works are obtained with the help of Cadence software. Table 2 shows the model parameters of CNTFET.

4.1 Simulation result and parameters analysis of traditional 4:2 compressor using two complete full adders

The operating voltage of 0.9 V is applied to the input pins, and the output waveform is obtained from the Carry and Sum. The resultant waveform is shown in Fig. 6, and the propagation delay factor and the EDP and PDP values are tabulated in Table 2 for varying voltages from 0.7 to 1.1 V. Due to the increase in the biasing voltage, the power and delay values also increase. In the waveform, A, B, C, D, and CIN are the five inputs for the compressor, and the variables X and Y represent sum and carry, respectively. Other than sum and carry, another output called COUT is obtained. From the Table 3, it is found that the propagation delay value is approximately equal at various values between 0.7 and 1.1 V. Increased power and delay values result in increased PDP and EDP values.

4.2 Simulation result and parameters analysis of 4:2 compressor using two pseudo half adders

The operating voltage of 0.9 V is applied to the input, and the resultant waveform is obtained from Carry and Sum. The output waveform is shown in Fig. 7. The performance metrics are tabulated in Table 3 at various values between 0.7 and 1.1 V.

Due to the increase in the supply voltage, the power and delay values also increase. In the waveform, A, B, C, D and Cin are the five inputs for the compressor, and the output variables are represented by Sum, Carry, and Cout, respectively. From the Table 4, it is found that the propagation delay value is approximately equal at various values between 0.7 and 1.1 V. Increased power and delay values result in increased PDP and EDP values.

Table 2 The CNTFET design, process, or model parameters

Parameter	Typical value (32 nm)
Technology Node	32 nm
Channel Material	Single-walled CNT (SWCNT)
Channel Diameter	1–2 nm
Chirality (nm)	(10,10)
Channel Length (L)	32 nm
Gate Oxide Thickness (tox)	2 nm
Gate Material	HfO2 (high-k)
Threshold Voltage (Vth)	0.2–0.3 V
Carrier Mobility (μ)	1000–4000 $cm^2/V{\cdot}s$
Gate Capacitance (Cox)	10–20 $fF/\mu m^2$
Contact Resistance (Rc)	10^{-6} to 10^{-7} Ω·μm
Subthreshold Slope (SS)	~60 mV/decade
Switching Speed (ft)	300–500 GHz

4.3 Simulation result and parameter analysis of 4:2 compressor using three input majority gate

The operating voltage of 0.9 V is applied to the input pins, and the output waveform is obtained from the Carry and Sum. The output waveform is shown in Fig. 8. The performance metrics are tabulated in Table 4 at various voltage values between 0.7 and 1.1 V. Due to the increase in the supply voltage, the power and delay values also increase. In the waveform, A, B, C, D and Cin are the five inputs for the compressor, and the output variables are represented by Sum, Carry, and Cout, respectively. From the Table 5, it is found that the propagation delay value is approximately equal at different voltages. Increased power and delay values result in increased PDP and EDP values. Comparing the power and propagation delay values of the existing models 1 and 2, the output result obtained for the 4:2 compressor using a three-input majority gate is comparatively low.

4.4 Simulation result and parameter analysis of proposed 4:2 compressor design

The resultant waveform as shown in Fig. 9. The performance analyses are tabulated in Table 5. In the waveform, A, B, C, D and Cin are the five inputs for the compressor, and the variables X and Y represent sum and carry, respectively. Other than sum and carry, another output called COUT is obtained. From the Table 6, it is found that the propagation delay value is constant at various voltage values between 0.7 and 1.1 V. Increased power values result in increased PDP and EDP values. Comparing the power and propagation delay values of the existing models 1, 2 and 3, the output result obtained for the proposed 4:2 compressor using a 2×1 multiplexer is comparatively low.

4.5 Comparison of performance metrics among existing and proposed model

Table 7 represents the comparison among the models. The performance metrics have been analyzed. The average values of the obtained results of existing and proposed models are tabulated. The table confirms that the proposed structure is more effective than the methods currently in use.

From the graphs of power, delay, PDP, and EDP, it is found that the 4:2 compressor using two pseudo-half adders (existing model 2) shows a larger value comparatively than the other models. There are 68 transistors in the existing Model 2. An increased power value and output delay are caused by an increased transistor count [31].

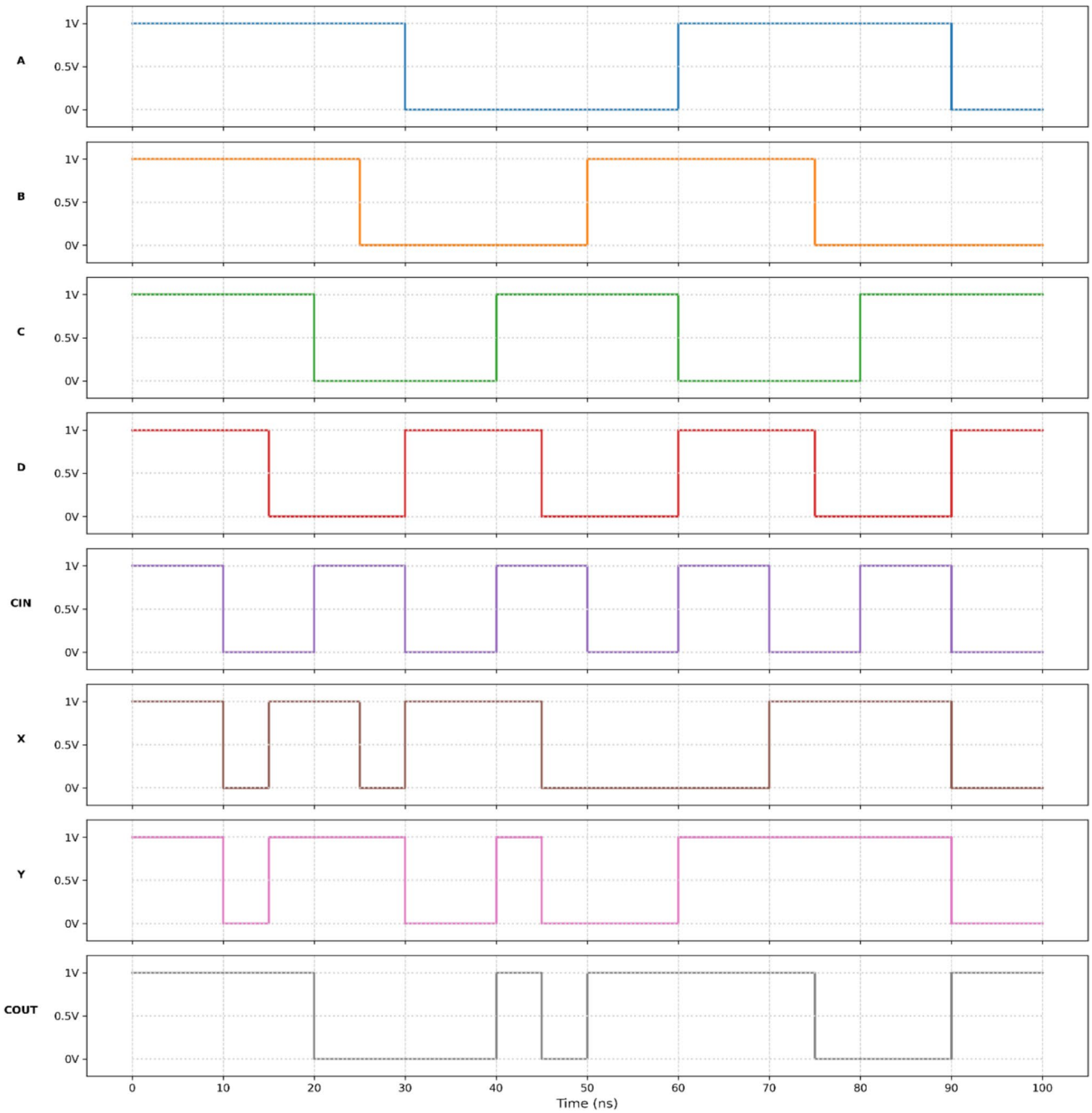


Fig. 6 Simulation result of 4:2 compressor using two complete full adders

Table 3 Parameter analysis of 4:2 compressor using two complete full adders

Voltage (V)	Power (Microwatts)	Propagation delay (femto Seconds)	Power delay product (femto Joules)	Energy delay product (Joules Seconds) (10^{-30})
0.7	0.347	16.18	5.614	90.83
0.8	0.396	16.19	6.420	103.93
0.9	0.446	16.19	7.222	116.92
1.0	0.594	16.19	9.621	155.76
1.1	0.653	16.19	10.581	171.30

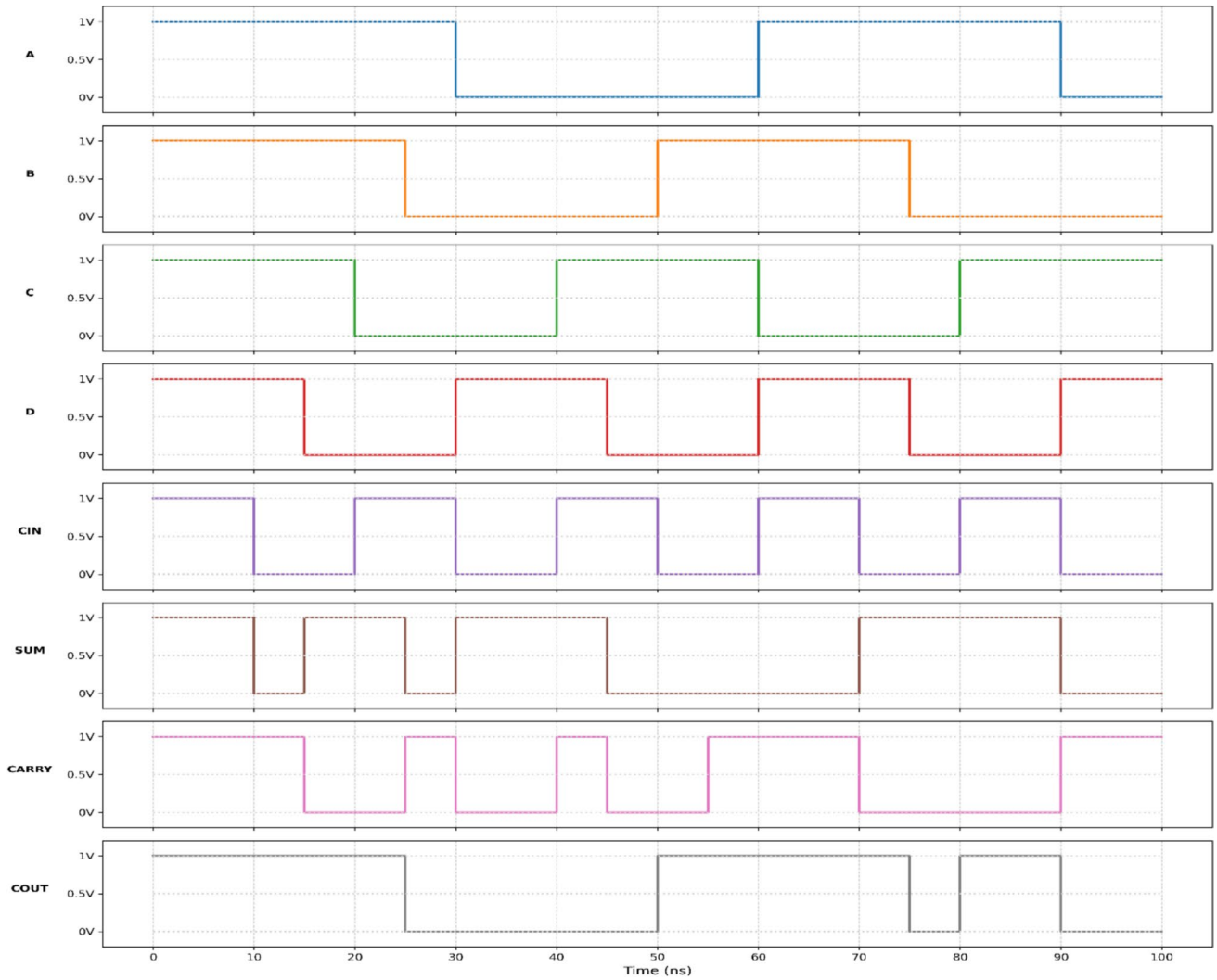


Fig. 7 Simulation result of 4:2 compressor using two pseudo half adders

Table 4 Power, delay, PDP and EDP of 4:2 compressor using two pseudo half adders

Voltage (V)	Power (Microwatts)	Propagation delay (femto Seconds)	Power delay product (femto Joules)	Energy delay product (Joules Seconds) (10^{-30})
0.7	0.490	20.25	9.938	201.24
0.8	0.892	20.25	18.081	366.14
0.9	0.631	20.26	12.784	259
1.0	0.701	20.27	14.211	288
1.1	0.771	20.25	15.616	316.22

4.6 MONTE CARLO analysis for existing and proposed model

The Monte Carlo analysis for the 4:2 compressor using full adders (Existing Model 1) is done and tabulated as shown in Table 8. In addition, the mean and standard deviation of power for the existing models are given in Figs. 10, 11, and 12.

The Monte Carlo analysis for 4:2 Compressor using two 2×1 Multiplexer (Proposed Model) is done and tabulated in the Table 9. The mean value and the standard deviation of power and delay for the proposed model which operating at a of 0.9 V, is displayed in the Figs. 13, 14 and 15.

Nanoscale designs are stable, as evidenced by the power and delay values, which show accurate and consistent measurements with zero standard deviation. The simulation's

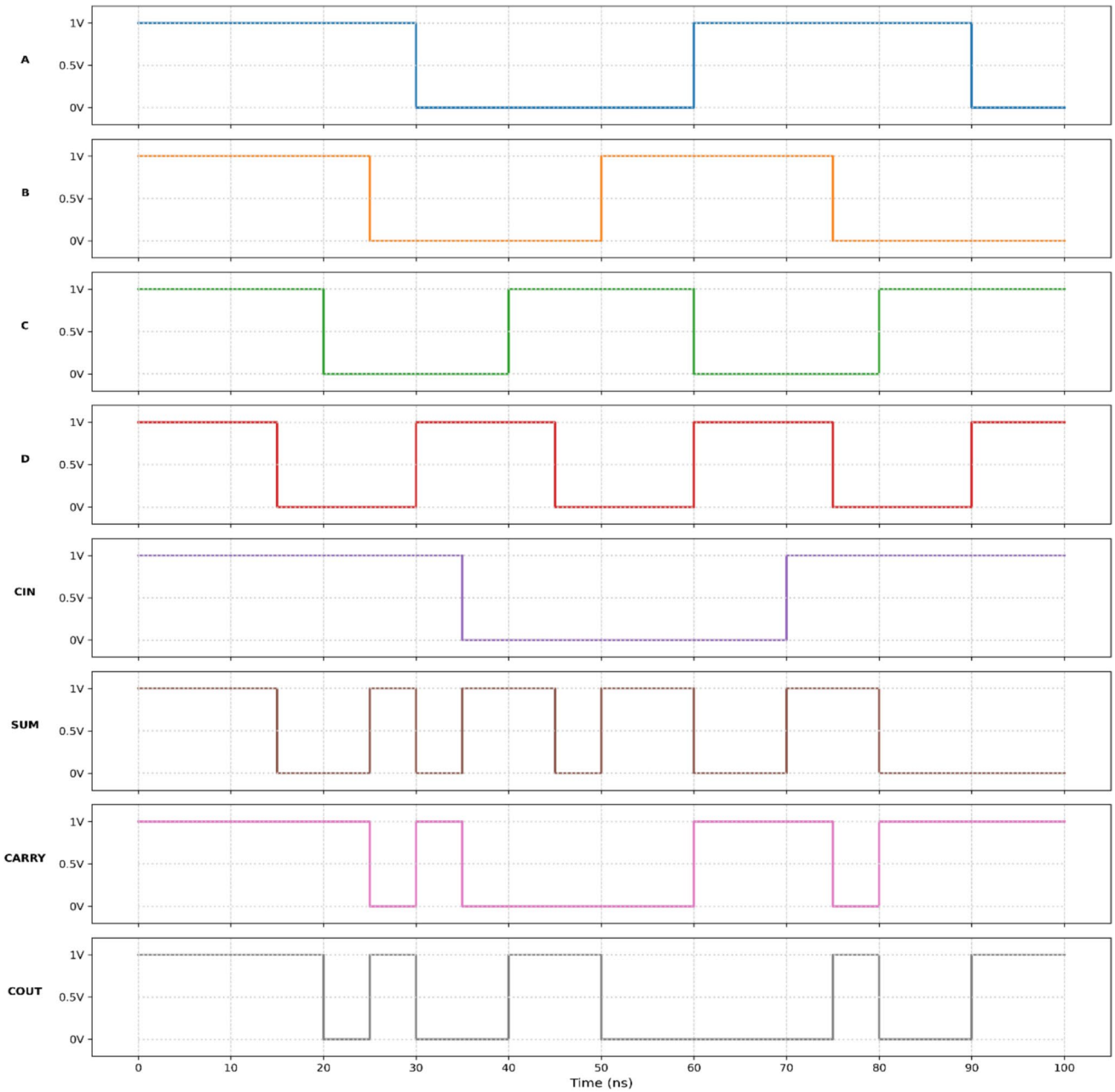


Fig. 8 Simulation output of 4:2 compressor using three input majority gate

Table 5 Parameter results of 4:2 compressor using three input majority gate

Voltage (V)	Power (Micro Watts)	Propagation delay (femto Seconds)	Power delay product (femto Joules)	Energy delay product (Joules Seconds) (10^{-30})
0.7	0.384	15.22	5.853	89.14
0.8	0.439	15.22	6.681	101.75
0.9	0.494	15.23	7.531	114.69
1.0	0.549	15.23	8.367	127.42
1.1	0.604	15.23	9.205	140.19

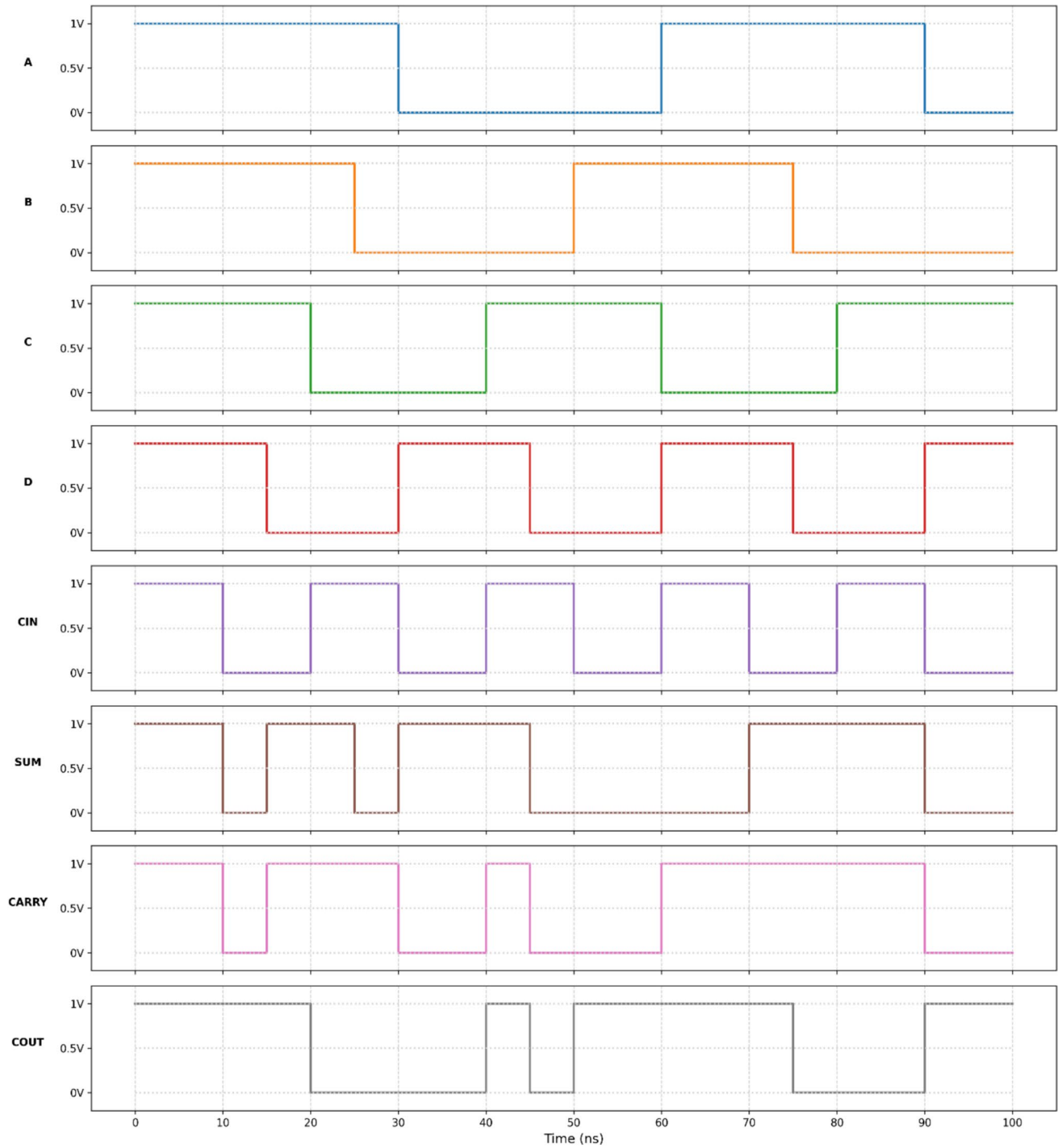


Fig. 9 Output waveform results of proposed 4:2 compressor using 2 × 1 Mux

waveform alignment is the cause of the negative delay figures, which don't point to performance problems.

The overall efficiencies for the proposed and existing models are calculated. In the dynamic power, when comparing the planned model with the standing models (1, 2, and 3), the results show a reduction of power to 35.9%, 9.60%, and 8.32%, respectively. Following that, when comparing the proposed model with the existing models (1, 2, and 3), the delay is reduced to 24.9%, 0.06%, and 5.99%, respectively. In EDP, when comparing the proposed model with the existing models (1, 2, and 3), the results of the reduction of EDP are 63.32%, 9.67%, and 18.97%, respectively. In the result of PDP, when comparing the proposed model with the existing models (1, 2, and 3), they are reduced to 51.85%,

Table 6 Power, delay, PDP and EDP analysis of proposed 4:2 compressor

Voltage (V)	Power (Micro Watts)	Propagation delay (femto Seconds)	Power delay product (Femto Joules)	Energy delay product (Joules Seconds) (10^{-30})
0.7	0.384	15.22	5.850	89.00
0.8	0.439	15.22	6.687	101.77
0.9	0.494	15.22	7.521	114.46
1.0	0.549	15.22	8.357	127.19
1.1	0.367	15.22	5.593	85.12

Table 7 Comparative parametric analysis of existing and proposed models

Performance parameter	Existing 1 (Ref 19)	Existing 2 (Ref 19)	Existing 3 (Ref 19)	Proposed
Power (Microwatts)	0.4876	0.6974	0.4944	0.4469
Delay (femto Seconds)	16.19	20.26	15.23	15.22
Power delay product (femto Joules)	7.90	14.13	7.527	6.801
Energy delay product (Joules Seconds)10^{-30}	127.75	286.12	114.6	103.51

Table 8 Monte Carlo analysis for 4:2 compressor using two full adders

Parameter	Mean	Std. deviation
Power(W)	446.090 m	6.66400n
Delay(S)—Rising	− 30.3720n	0.0
Delay(S)—Falling	− 15.4847p	335.928z

9.64%, and 13.8%, respectively. The overall average of the design in power is 17.94%; the delay is 10.31%; the EDP is 30.82%; and the PDP is 25.09%.

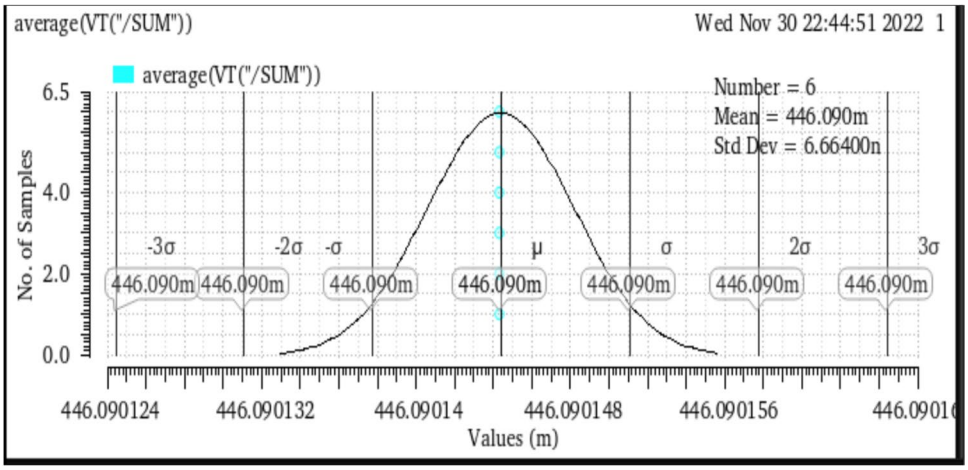


Fig. 10 Mean and standard deviation for power (existing model 1)

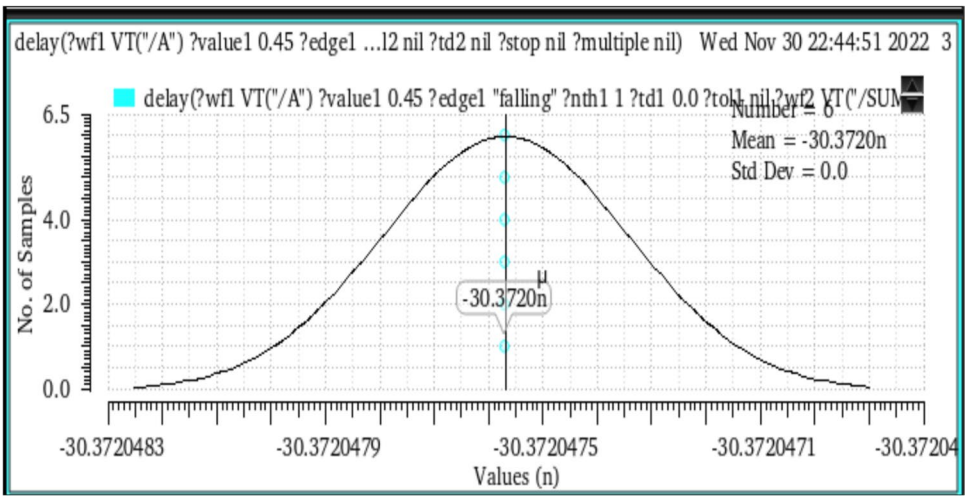


Fig. 11 Mean and standard deviation for rising delay (existing model 1)

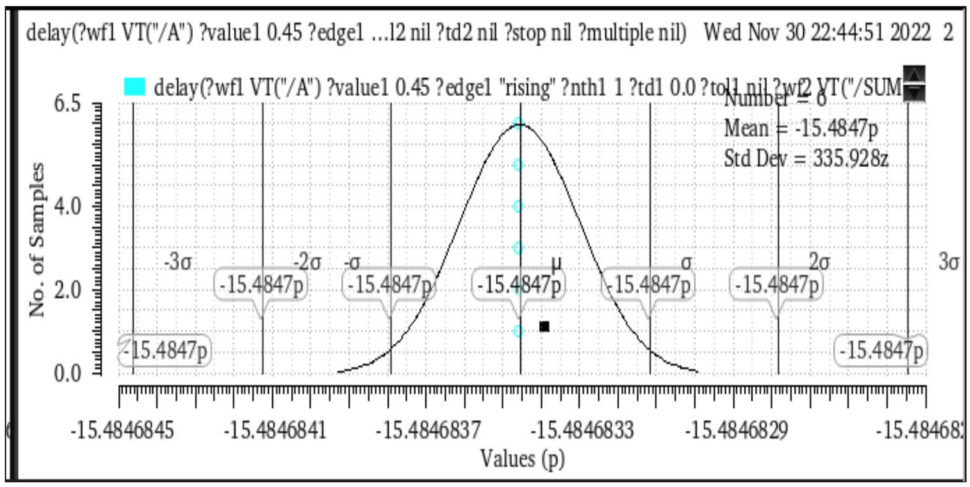


Fig. 12 Mean and standard deviation for falling delay (existing model 1)

Table 9 Monte Carlo parameter analysis for proposed 4:2 compressor

Parameter	Mean	Std. deviation
Power (W)	494.180 m	0.0
Delay(S)—Rising	− 64.9670p	0.0
Delay(S)—Falling	− 30.3938p	0.0

5 Conclusion

The multiplier circuits commonly incorporate compressor circuits. In DSP systems, multipliers are a crucial and significant component. If effective, low power multipliers are used, the effectiveness of the DSP systems is improved. Based on power and delay reduction, this study suggests an effective low-power 4:2 compressor. Existing methods are used to generate the compressor circuit models that already exist. The main goals of the suggested 4:2 compressor design are the reduction of power consumption and EDP. The performance parameters of the suggested compressor are studied at 32 nm CNTFET and compared to existing designs. The suggested 4:2 compressors main objective is to reduce power usage, PDP, and EDP. The performance metrics of the proposed 4:2 compressor are superior to those

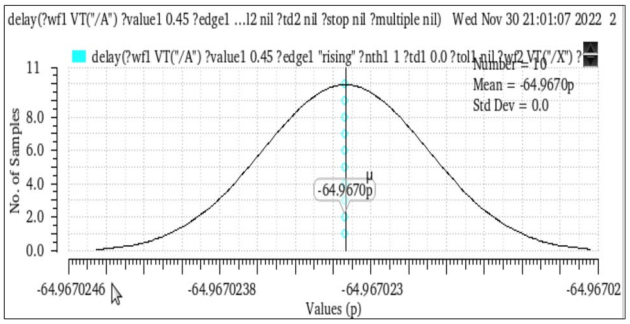


Fig. 14 Mean and standard deviation for rising delay (proposed model)

of the earlier compressor architectures. The simulation's findings show that the various effects of the suggested compressor's process modifications have less of an impact. The different methods of existing and proposed designs of 4:2 compressors are designed and executed using the Cadence Virtuoso tool. Apart from these, Monte Carlo analysis is also done, which helps find the mean value of the power and standard deviation. Further improvement of the compressor is also done using various low-power techniques, but this also affects the efficiency of the output. Any combination of

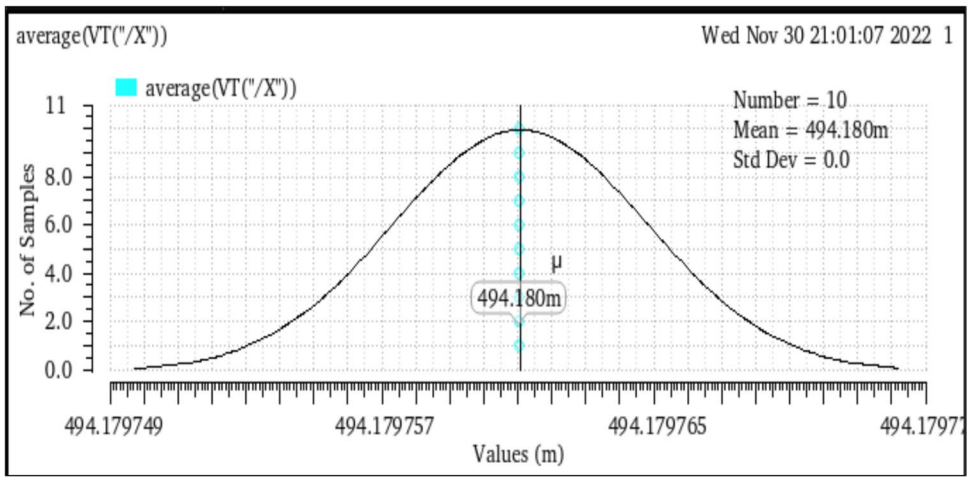


Fig. 13 Mean and standard deviation for power (proposed model)

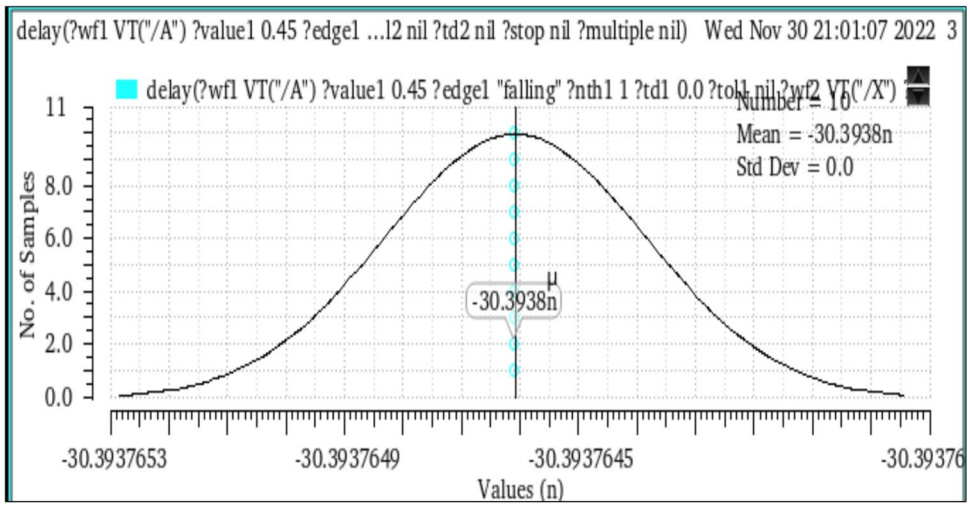


Fig. 15 >Mean and standard deviation for falling delay (proposed model)

area, power, and speed has to be compensated to provide an efficient 4:2 compressor.

Author contributions A (Gavaskar K): Conceptualization, Methodology, Writing—Original Draft, Supervision B (Elango S): Data Curation, Formal Analysis, Investigation C (Gopinath P): Software, Validation, Visualization D (Adhithyaa N): Writing—Review & Editing, Resources E (Srinath A): Project Administration, Funding Acquisition, Review & Editing.

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Code availability Not applicable.

Declarations

Competing interests The authors declare no competing interests.

Consent to participate Quality publication.

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